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A 6.16Gb/s 4.7pJ/bit/iteration LDPC decoder for IEEE 802.11ad standard in 40nm LP-CMOS

Hiroyuki Motozuka, Naoya Yosoku, Takenori Sakamoto, Takayuki Tsukizawa, Naganori Shirakata and Koji Takinami
Panasonic Corporation

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Outline

- Background
- Overview of LDPC decoding for IEEE802.11ad
- Proposed low power architecture
  - Column-parallel architecture for IEEE802.11ad
  - Low complexity variable cyclic shifters
- Experiment results
- Conclusion

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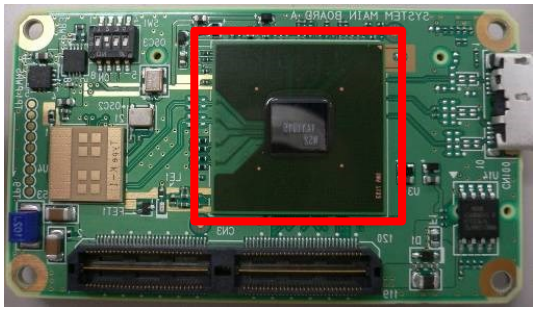
Background

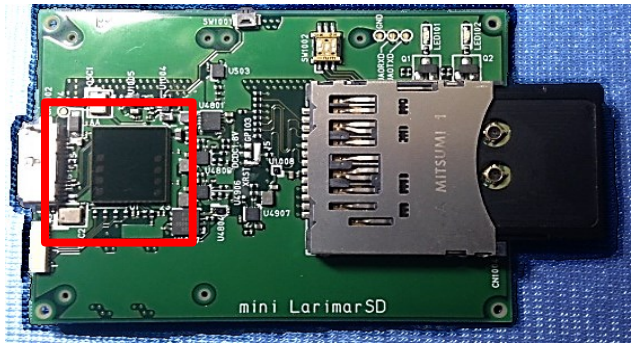
- IEEE802.11ad – 60 GHz band multi-gigabit wireless
- For mobile, challenge is power consumption
- LDPC decoder is one of the most power-hungry blocks

Achieve low power by improving LDPC decoder architecture

Previous work [1]
2.50 Gb/s
(3.08 Gb/s uncoded)



This work
4.62 Gb/s
(6.16 Gb/s uncoded)



[1] Tsukizawa, et al, ISSCC 2013

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LDPC matrices in IEEE802.11ad

- Four matrices for different code rates
- Consist of cyclic shift sub-matrices

Rate 1/2

40		38		13		5		18							
34															
	36														
	27														
35															
29															
	31														
	22														

Rate 5/8

20	36	34	31	20	7	41	34		10	41					
30	27														
35															
29															
	31														
	22														

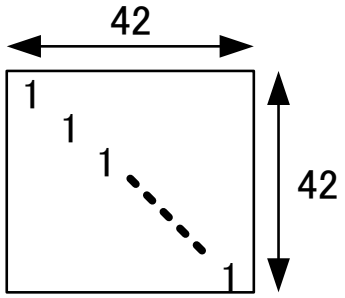
Rate 3/4

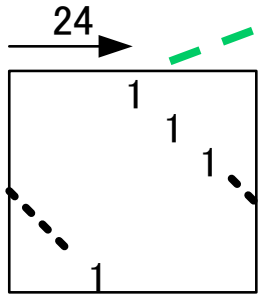
35	19														
29	30														
37	31														
25	22														

Rate 13/16

29	30	0	8	33	22	17	4	27	28	20	27	24	23		
37	31	18	23	11	21	6	20	32	9	12	29		0	13	
25	22	4	34	31	3	14	15	4		14	18	13	13	22	24

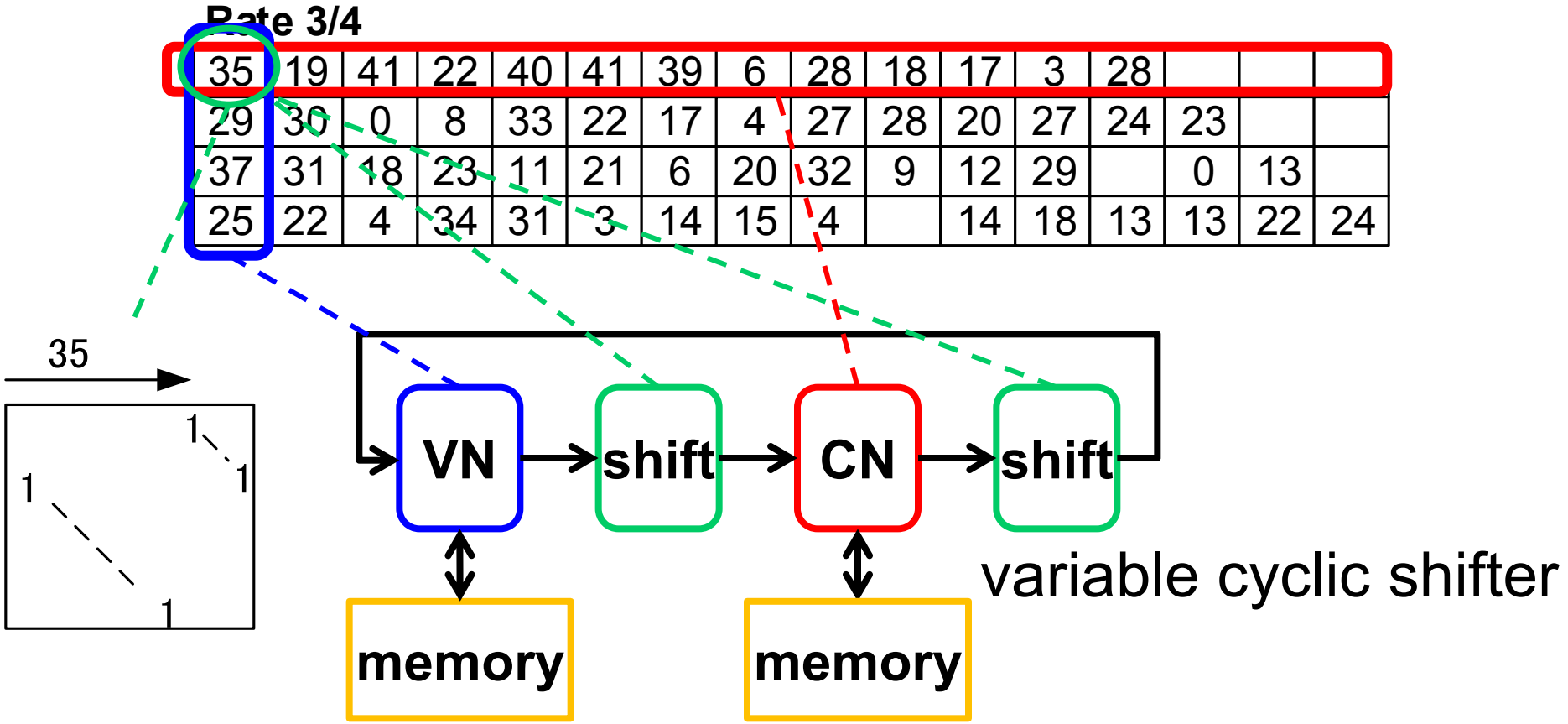
Sub-matrix





Min-Sum algorithm

- Min-Sum algorithm
  - Variable-Node processing (VN) – column by column
  - Check-Node processing (CN) – row by row



Parallel decoder architectures

- Parallel processing is required to achieve very high data rate – 6.16 Gb/s

Row-parallel – conventionally used for 11ad [2-4]

35	19	41	22	40	41	39	6	28	18	17	3	28			
29	30	0	8	33	22	17	4	27	28	20	27	24	23		
37	31	18	23	11	21	6	20	32	9	12	29		0	13	
25	22	4	34	31	3	14	15	4		14	18	13	13	22	24

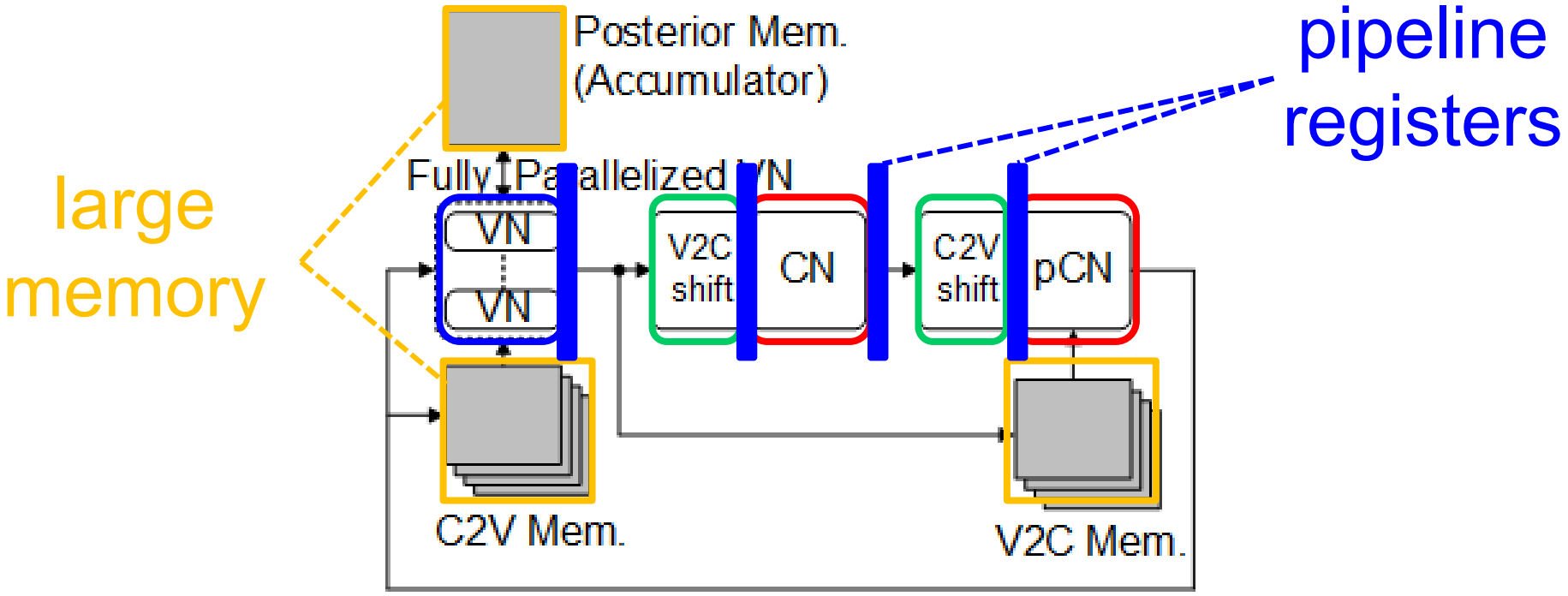
Column-parallel

35	19	41	22	40	41	39	6	28	18	17	3	28			
29	30	0	8	33	22	17	4	27	28	20	27	24	23		
37	31	18	23	11	21	6	20	32	9	12	29		0	13	
25	22	4	34	31	3	14	15	4		14	18	13	13	22	24

[2] Park, JSSC 2014
[3] Weiner, ISSCC 2014
[4] Li, SiPS 2013

Conventional row-parallel architecture

- Memory and pipeline registers dominate the power consumption
  - Parallelized VNs require large working memory



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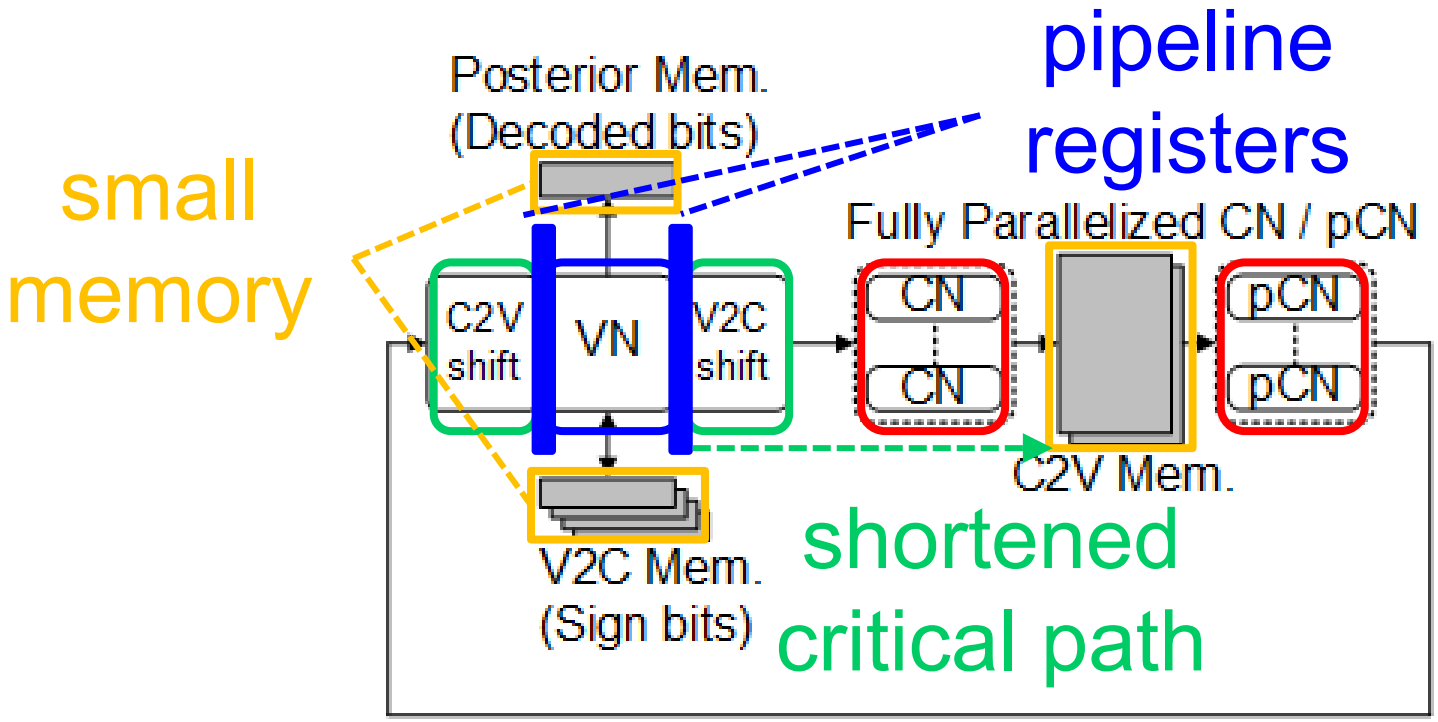
Proposed architecture – Overview

- Column-parallel architecture for IEEE802.11ad
  - Reduce memory size
- Low complexity variable cyclic shifters
  - Shorten critical path, and reduce pipeline registers



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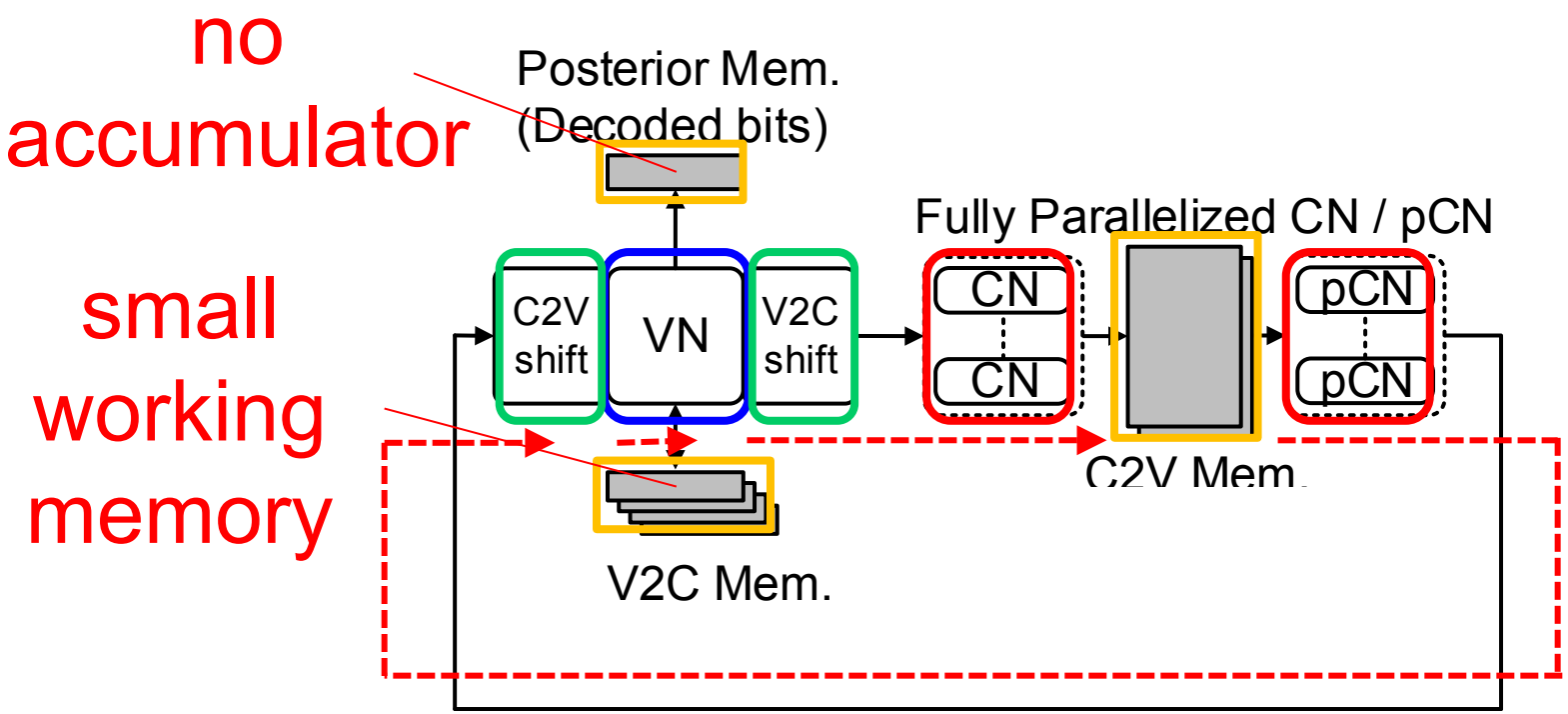
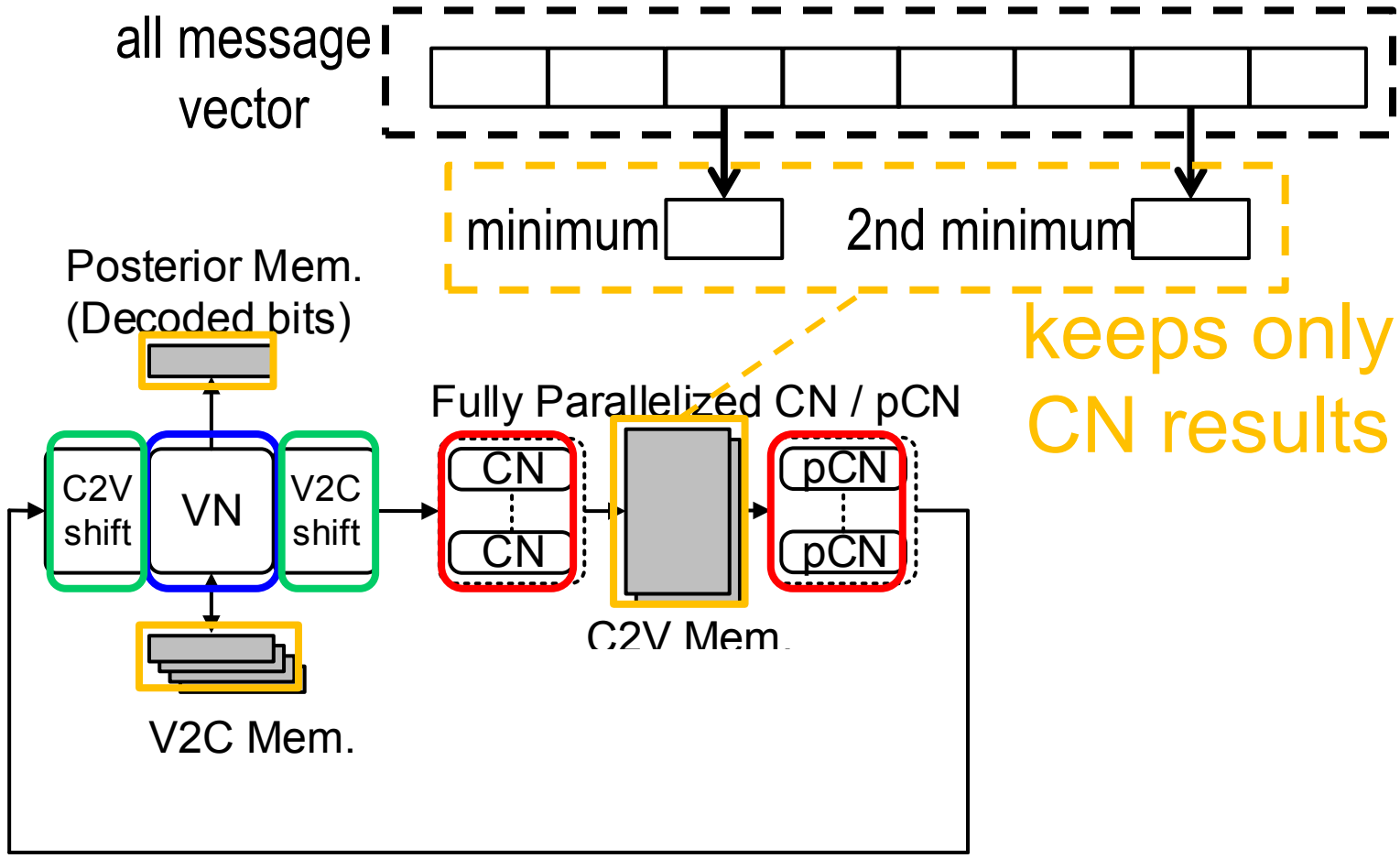
Proposed column-parallel architecture

- Data flows “one way” without large working memory nor accumulators
- Small working memory for VN processing



Proposed column-parallel architecture

- C2V memory only needs to keep CN results instead of all C2V messages



Memory size comparison

- Reduces memory bits by 60%
- Memory size reduction directly contributes to power reduction

Comparison of Memory Size

	Park JSSC 2014	**Weiner ISSCC2014**	**This work**
Architecture	Row-parallel	Row-parallel with approximation	Column-parallel
Implementation	eDRAM, Flip-Flop	Flip-Flop	Flip-Flop
Total bits	30240	20832	12096
Reduction		-31%	-60%

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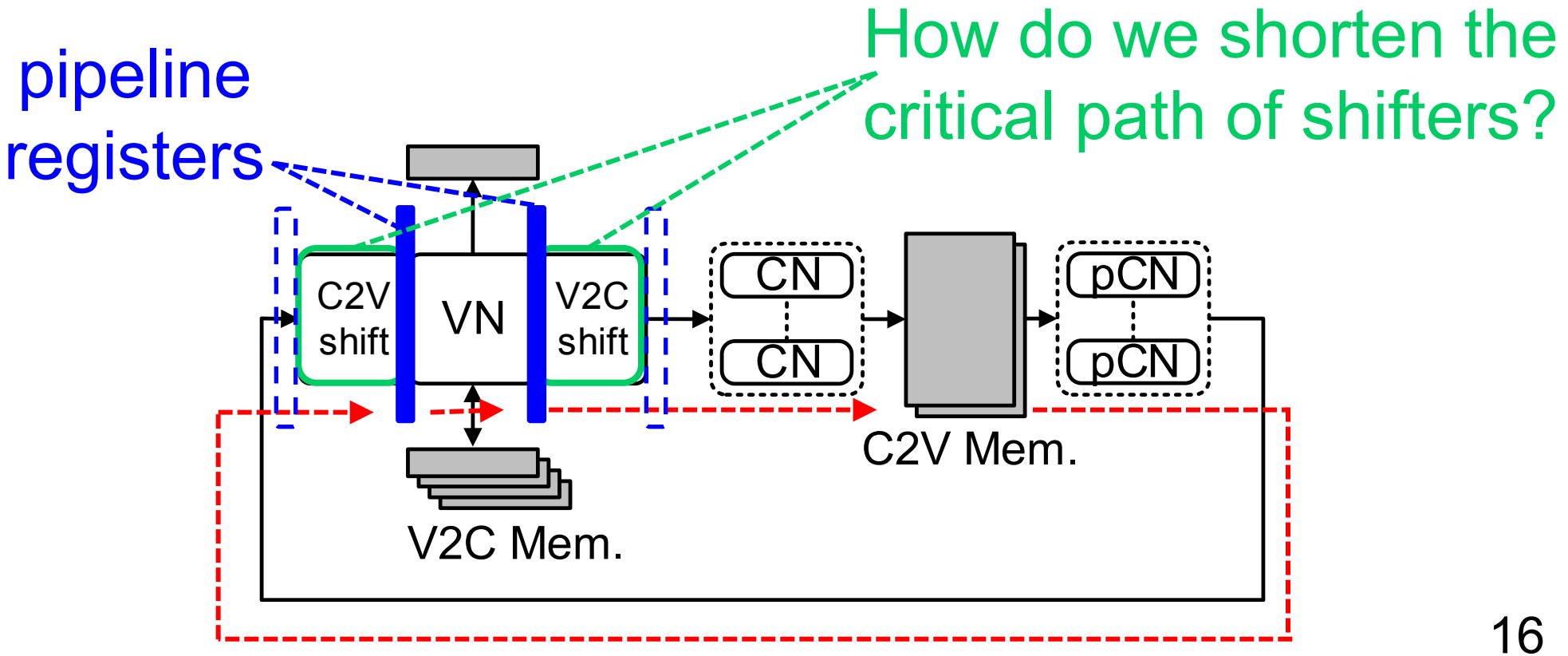
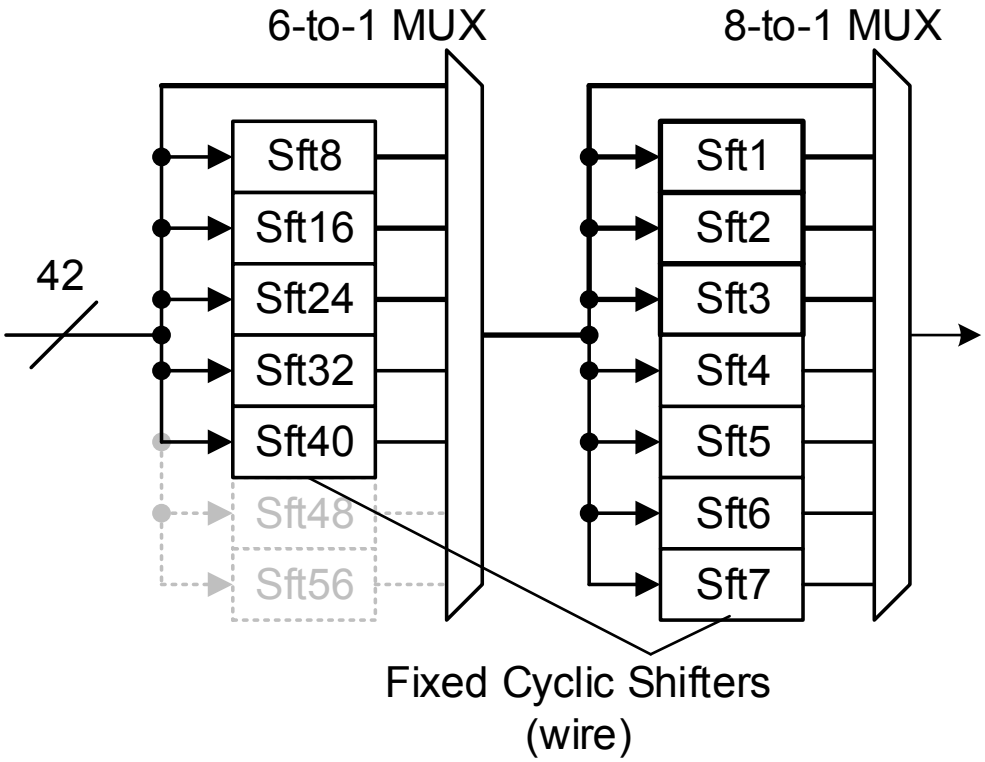
Reduce power on pipeline register

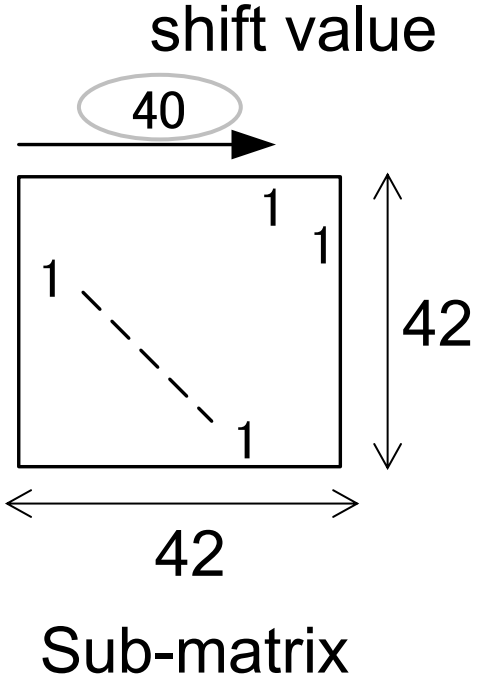
- By shortening critical path, we could reduce pipeline stages to three while achieving high speed processing
  - conventionally 4 – 5 stages



Conventional variable cyclic shifter

- Variable shifters can be implemented as barrel shifters
- Possible shift values: 0 to 41

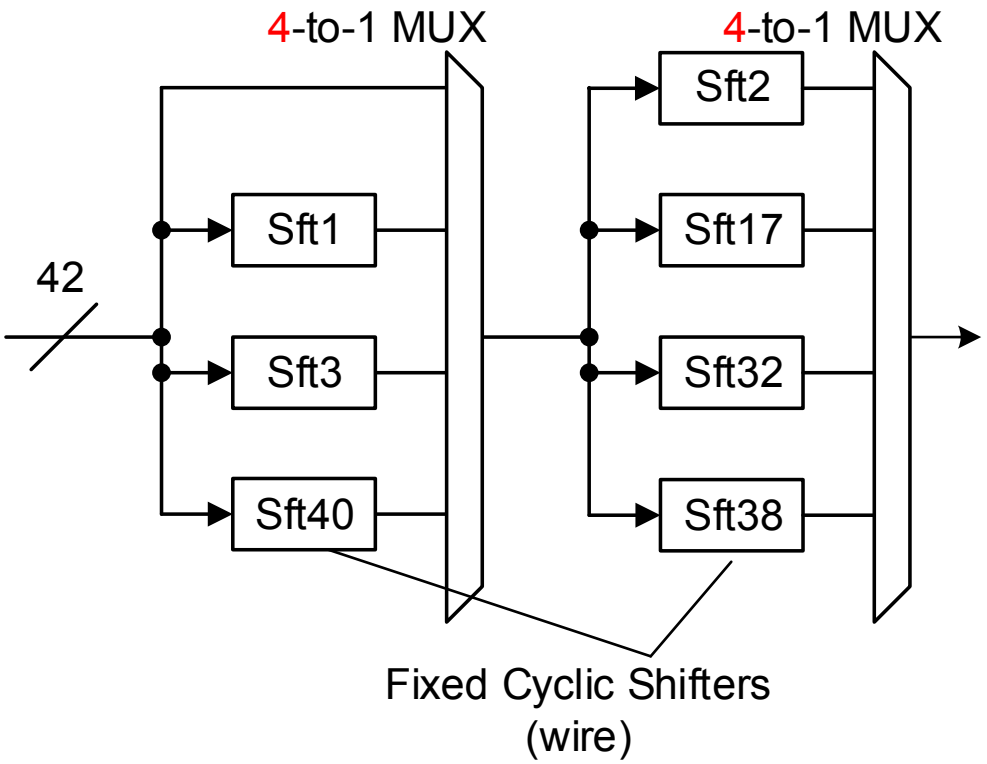




Radix-8 barrel shifter

Low complexity variable cyclic shifters

- The number of required shift values is limited to 9 – 13 for each shifter
- Utilize modulo addition



Proposed shifter

12 shift values

40 = (38+ 2) mod 42
38 = (0 +38) mod 42
13 = (38+17) mod 42
5 = (3 + 2) mod 42
18 = (1 +17) mod 42
41 = (3 +38) mod 42
20 = (3 +17) mod 42
34 = (38+38) mod 42
35 = (3 +32) mod 42
39 = (1 +38) mod 42
28 = (38+32) mod 42
17 = (0 +17) mod 42

Rate 1/2
Rate 5/8
Rate 3/4, 13/16

42% reduction of complexity

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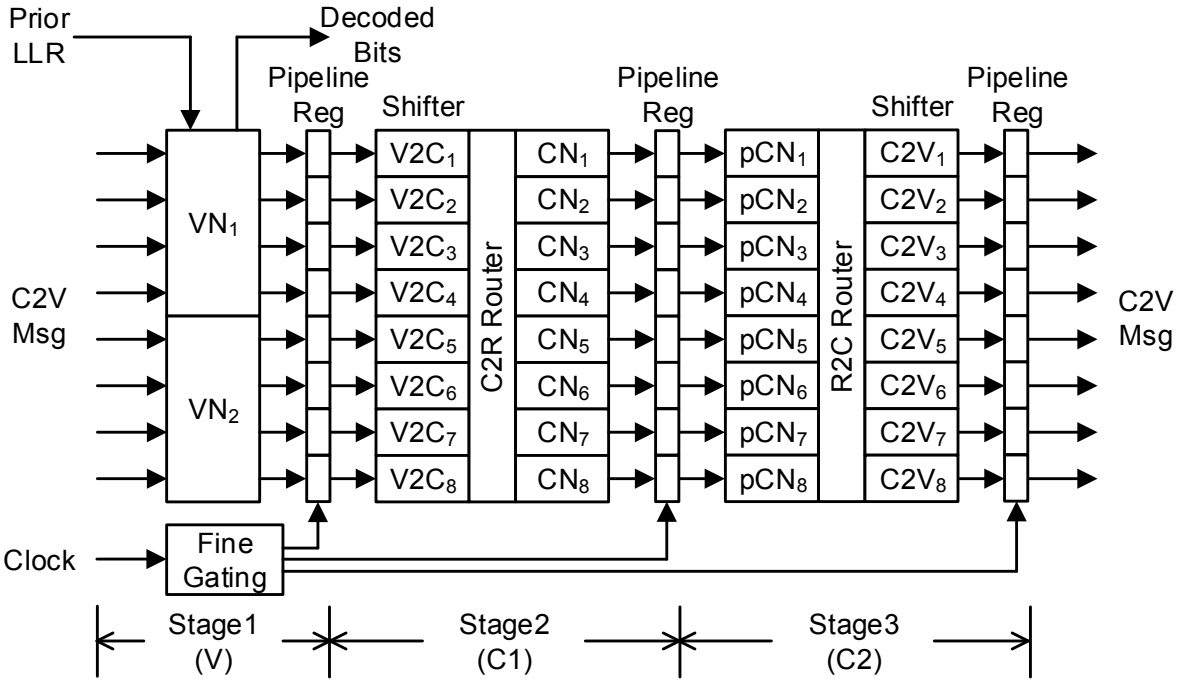
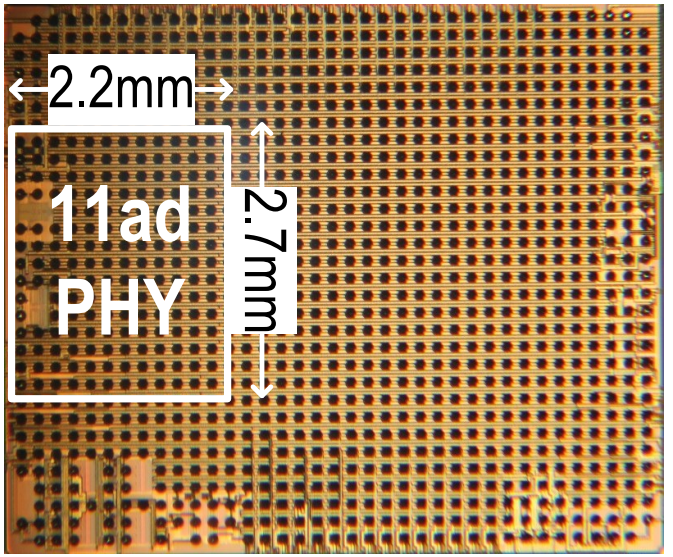
Prototype chip

- Fabricated in 40nm CMOS process
- Achieve uncoded 6.16Gb/s
  - Maximum data rate in 11ad SC PHY



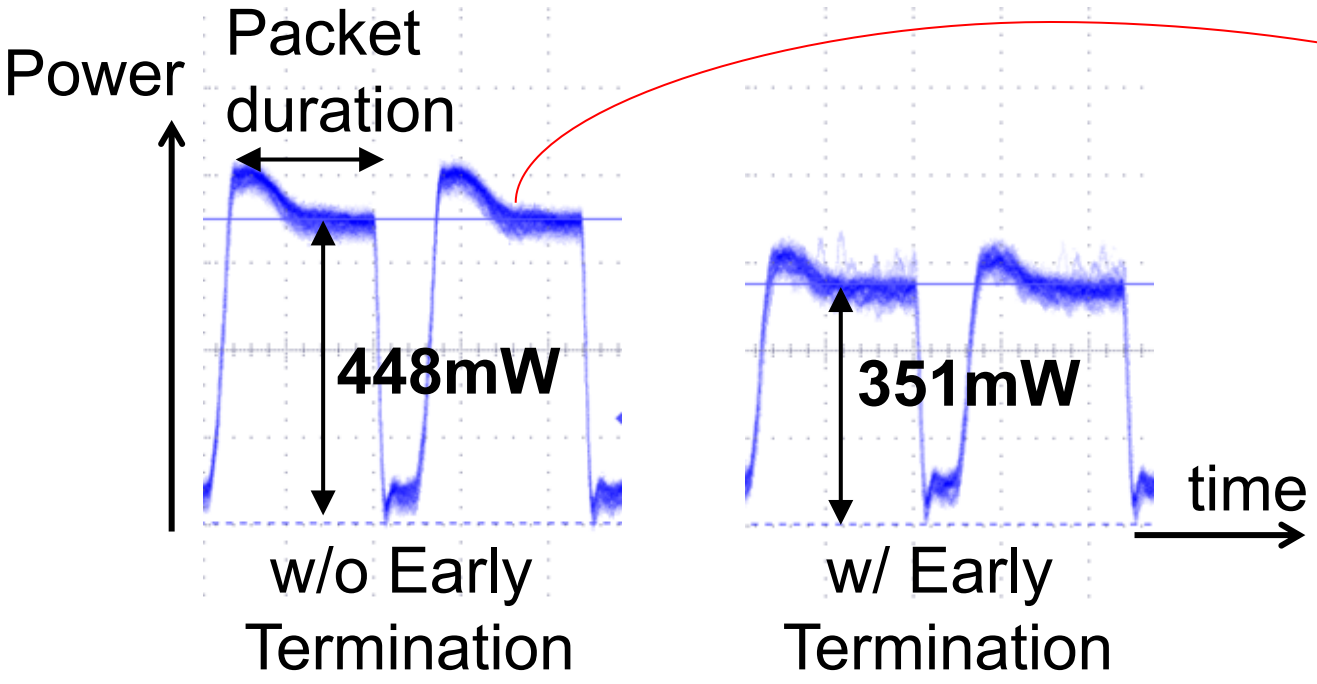
Designed LDPC decoder core



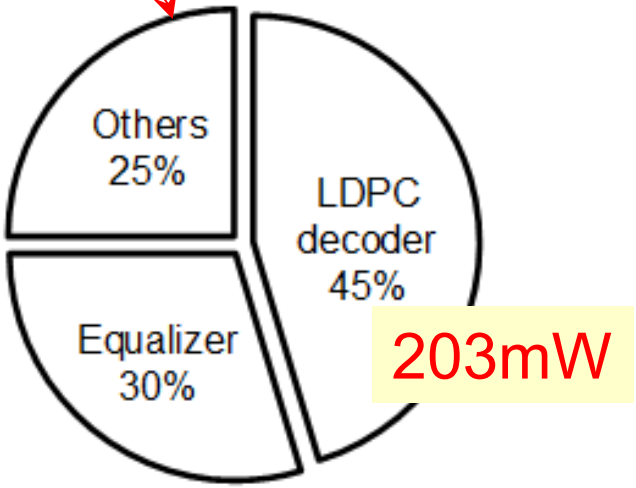
Die micrograph

Experiment Results

- Power consumption
  - Measured with fabricated chip
  - 203mW for 6.16Gb/s (16QAM, R=1/2)



Measured power consumption of PHY digital baseband

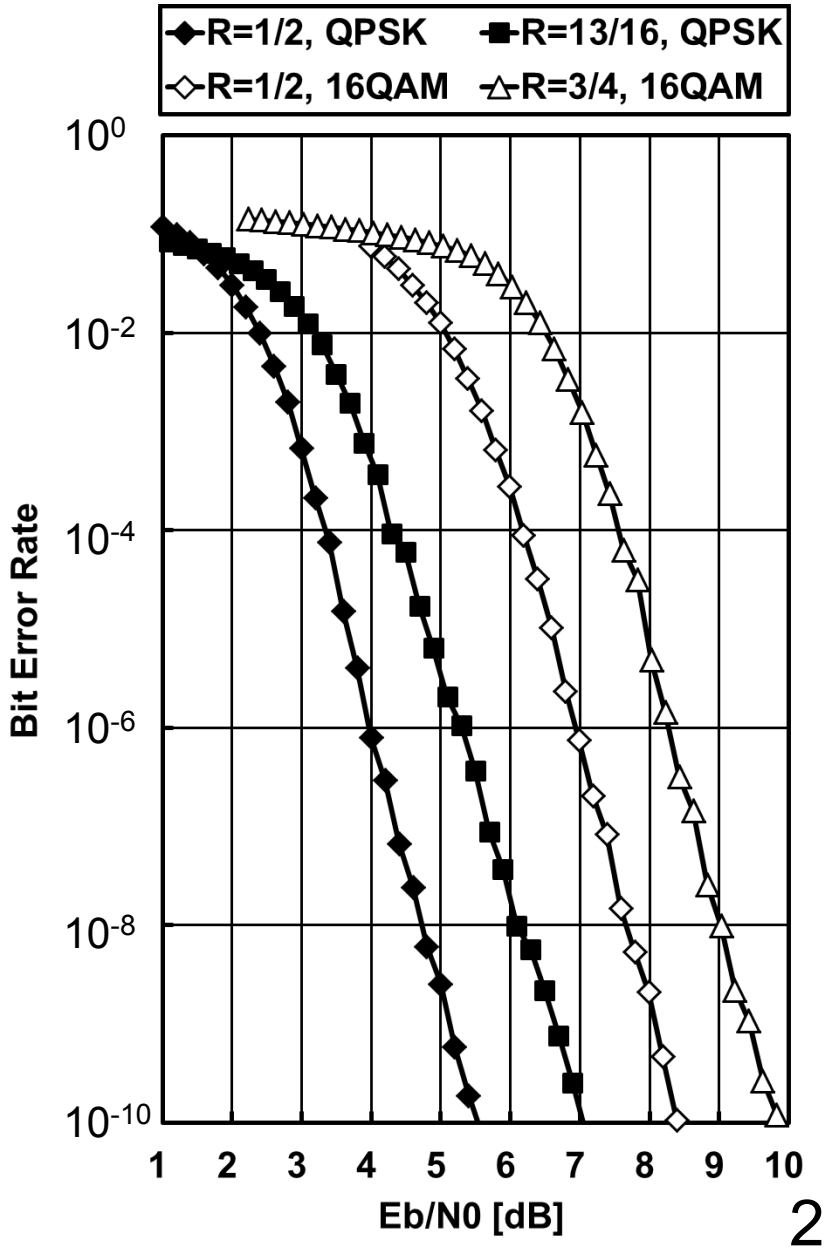


Power breakdown of PHY digital baseband

Experiment Results

- BER Performance
  - Error floor was not observed down to 10^{-10}
  - 11ad performance requirements are satisfied with 7 iterations

Simulation Parameters	
Channel Model	AWGN
Maximum number of iterations	7
Number of bits of Input LLR	5



Performance comparison

- This work achieves the lowest normalized energy efficiency of 4.7 pJ/bit/iteration besides it achieves best BER performance

	This work	Weiner ISSCC2014	Li SiPS2013
CMOS Technology	40nm LP	28nm FDSOI	40nm G
Supply Voltage	1.1	1.07	0.9
Hardware Mapping	Column-parallel	Row-parallel	Half-row-parallel
Scheduling	Flooding	Flooding	Layered
Iterations	7	3.75	5
Throughput [Gb/s]	6.16	12	5.6
BER @Eb/N0=5dB, BPSK/QPSK	**$<10^{-8}$**	$<10^{-6}$	$<10^{-6}$
Normalized Energy Efficiency [pJ/bit/Iteration]	**4.7**	6.0	7.0

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Conclusion

- We propose a novel LDPC decoder architecture for IEEE802.11ad. It features:
  - Column-parallel architecture, which reduces required memory bits by 60%
  - Low complexity variable shifters, which reduces complexity by 42%
- Proposed decoder achieves:
  - Normalized energy efficiency of 4.7pJ/bit/iteration without significant BER performance degradation