REDUCED-COMPLEXITY TRELLIS MIN-MAX DECODER FOR NON-BINARY LDPC CODES

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Abstract

- A novel modified TEC-TMM algorithm and decoder architecture are proposed.
- Exchanged messages between CNU and VNU are significantly reduced.
- A layered decoder for (2304, 2048) NB-LDPC code over GF(16) is designed.
- Area reductions for CNU and whole decoder are 19.4% and 26.56%, respectively, with similar FER performance.

Introduction

- NB-LDPC codes outperform their binary counterparts in terms of error correction performance.
- Decoder architectures, especially CNU, have high complexity and large memory requirement.
- New algorithm and architectures are required to reduce the decoder area and improve the throughput.

Modified Two-Extra-Column Trellis Min-Max Algorithm

Algorithm 1 Modified TEC-TMM algorithm

Input: $\mathbf{Q_{mn}}, z_n = \arg\min_{a\in GF(q)} Q_{mn}(a); \forall n \in N(m)$

1: $\Delta Q_{mj}(\eta = a \oplus z_j) = Q_{mj}(a); (0 \le j < d_c)$

2: $\beta = \sum_{j=0}^{d_c-1} z_j \in GF(q)$

3: $\{m1(a), I(a)\} = \varphi\{\Delta Q_{mk}(a)|_{k=0}^{d_c-1}\}$

4: $\{\Delta Q'(a), d1(a), d2(a)\}$= $\min_{\eta'_k(a)\in conf(1,2)}\{\max_{k=1,2}(m1(\eta'_k(a)))\}$; $\Delta Q''(a) = \min 2_{\eta'_k(a)\in conf(1,2)}\{\max_{k=1,2}(m1(\eta'_k(a)))\}$

5: $\{\Delta Q'_{m1}, \Delta Q'_{m2}, a_{m1}, a_{m2}\} = \varphi'\{\Delta Q'(a)|_{a=1}^{q-1}\}$

Output: $\Delta Q'_{m1}, \Delta Q'_{m2}, a_{m1}, a_{m2}$; $\Delta Q''(a)$; $d1(a)$; $d2(a)$; $z_n^* = z_n \oplus \beta$

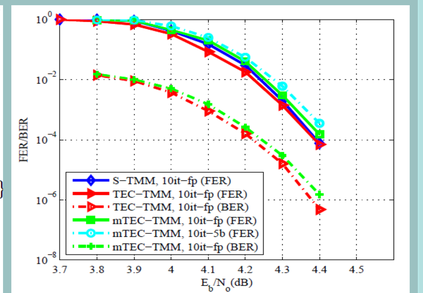

Fig. 1. FER and BER performance of (2304, 2048) NB-LDPC code over GF(16) under the AWGN channel.

- Two extra columns, ΔQ' **and** ΔQ'', including q elements are constructed based on only the first minimum values in each row.
- Only two elements with the smallest values in the first extra column ΔQ' are kept.
- The number of output elements is reduced.
- The remain ΔQ' elements are approximately calculated as $\Delta Q'(a) = \gamma \Delta Q'_{m2}$.

NB-LDPC Decoder Architecture

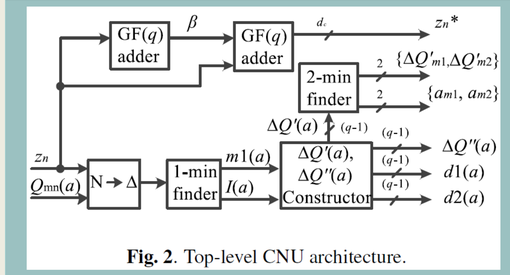

Fig. 2. Top-level CNU architecture.

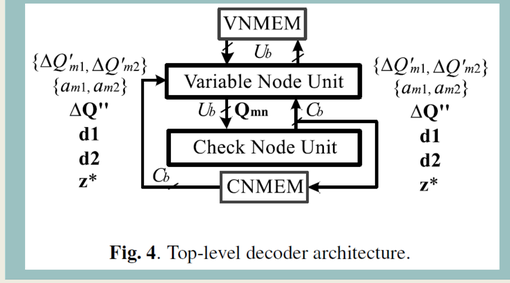

Fig. 4. Top-level decoder architecture.

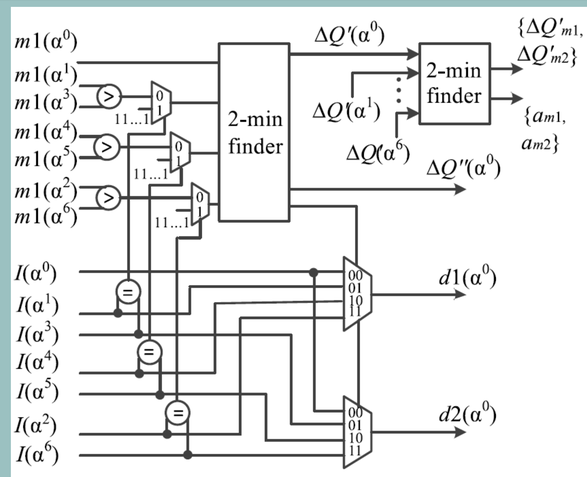

Fig. 3. Two extra column constructor for α^0 over GF(8).

- (q−1) 1-min finders with dc inputs are proposed to find the most reliable messages m1(a) instead of 2-min finders.
- Only one 2-min finder is proposed to find the first two minimum values $\Delta Q'_{m1}$, $\Delta Q'_{m2}$.
- The proposed CNU architecture significantly reduces the complexity because of using 1-min finder.
- CNU area is greatly reduced when increasing dc value.

Experimental Results

- Table 1 shows that the proposed CNU reduces gate count by 40.3% and exchanged bits by 85.5%, compared to [6].
- Compared to [9], gate count and exchange bits are reduced by 19.4% and 12%, respectively.

Table 1. CNU complexity comparison

GF(16), $d_c = 36$	[6]	[9]	Proposed
Gate count (NAND)	80.2K	59.4K	47.86K
Memory (bits)	2880	474	417
Quantization	5	5	5

- Table 2 shows that the proposed decoder greatly reduces gate count by 62% and 26.56%, compared to [6] and [9], respectively.
- Reducing both the CNU complexity and wiring congestion between CNU and VNU leads to a great improvement in the maximum frequency.
- Overall efficiency of the proposed decoder is almost twice as high as the one of the decoder in [9].

Table 2. Comparison of the proposed (2304, 2048) NB-LDPC layered decoder over GF(16) with other works

GF(16), $d_c = 36$	[6]	[9]	Proposed
Report	Post-layout	Post-layout	Synthesis
Technology	90-nm	90-nm	90-nm
Quantization	5	5	5
Gate count (NAND)	1882K	975K	716K
f_{clk}	330.8	333.3	433.8
Throughput (Mbps)	957.5	964.7	1396
Efficiency (Mbps/M gates)	508.8	989.4	1949.7

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