HIGH-ACCURACY STOCHASTIC COMPUTING-BASED FIR FILTER DESIGN

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Motivation

- Stochastic Computing (SC) requires low hardware complexity
- Attractive to resource constraint 5G IoT devices
- Generated probabilistically, SC design innately incurs errors.
- High-order SC FIR design is inherently error prone irrespective of the performance of individual SC module
- Recent works focus mainly on the performance of SC unit
- Room to improve performance by reducing the sources of SC errors.

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Contribution

- Identification of sources of errors for FIR filter that could be reduced
  - Higher number of SC processing blocks
  - Lower magnitude of SC value
- Reduction of the sources of errors
  - Reduction of number of SC processing blocks using Fast FIR Algorithm
  - Selectively picking higher magnitude of SC value
- Software implementation of FIR filter with highest-order not attempted before.
- Paving the way of promoting stochastic FIR in practical applications (higher-order)

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SC Background

- Derived from the conventional binary radix computing (BC), it represents any value by a stream of bits ('1's and '0's).
- Two modes:
  - Uni-polar; N-bit stream containing X bits of '1's where $x = P(X) = X/N$
  - Bi-polar; N-bit stream is presented by X bits of '1's where $x = 2(X/N)-1$
- A random number generator (RNG) generates a number which is then compared with the given BC value by a comparator, resulting in 1 or 0.
- This process is done iteratively to create a N-bit SC bit stream of 1's and 0's that reflects the SC value

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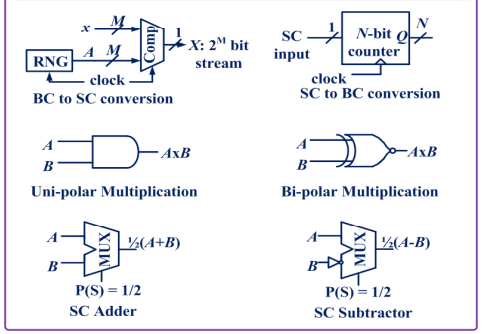
SC Background



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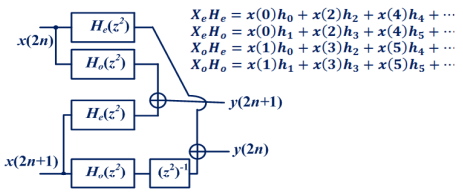
2-by-2 FFA(FFA2)

By using 2-by-2 FFA, a filter of order m can be reduced to 4 sub-filters of order $m/2$



$$X_eH_e = x(0)h_0 + x(2)h_2 + x(4)h_4 + \cdots$$
$$X_eH_o = x(0)h_1 + x(2)h_3 + x(4)h_5 + \cdots$$
$$X_oH_e = x(1)h_0 + x(3)h_2 + x(5)h_4 + \cdots$$
$$X_oH_o = x(1)h_1 + x(3)h_3 + x(5)h_5 + \cdots$$

Table 1. Mapping of a with h of H_e and H_o

General a parameters	a_1	a_2	...	$a_{m/2-1}$	$a_{m/2}$
Mapped H_e parameters	h_0	h_2	...	h_{m-4}	h_{m-2}
Mapped H_o parameters	h_{m-1}	h_{m-3}	...	h_3	h_1

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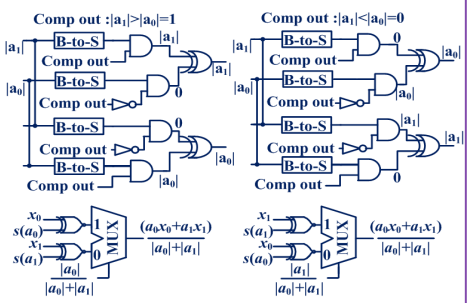
Selection of higher value



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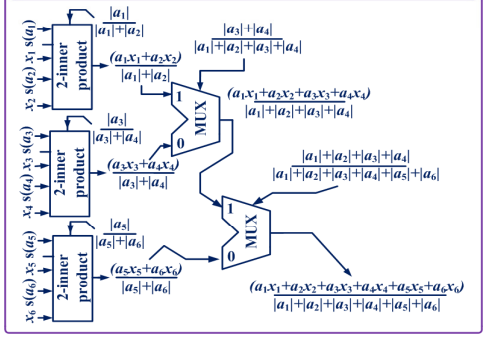
SC FFA2 FIR Filter (order 12)



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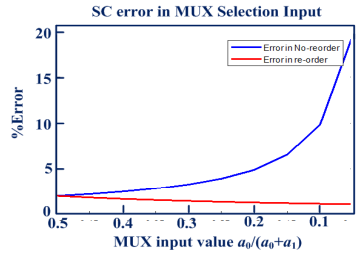
Error Performance



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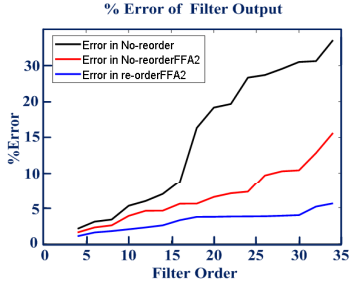
Error Performance



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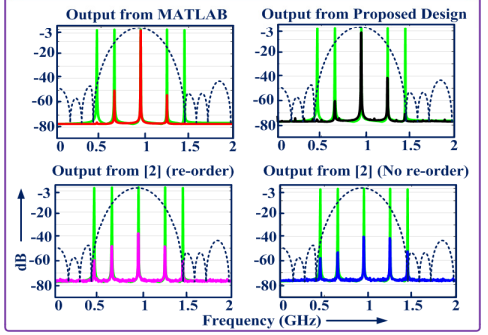
Simulation Results



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Summary

- We propose a new approach that addresses the errors of SC FIR filter and provide corresponding solution.
- We reduce the SC errors by lowering the number of SC processing blocks using 2-by-2 FFA.
- We also improve the SC error performance by swapping the h parameters to get higher value of MUX control input.
- Simulation results shows that the combination of these two error reduction approaches can significantly improve the performance compare to existing ones.
- In future we will design higher order FIR filter using higher parallelism of FFA such as FFA3, FFA6 etc.

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Reference

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