

APPROXIMATE BELIEF PROPAGATION DECODER FOR POLAR CODE {MENGHUI XU, SHUSEN JING, CHUAN ZHANG, JUN LIN, WEIKANG QIAN AND XIAOHU YOU } NATIONAL MOBILE COMMUNICATIONS RESEARCH LABORATORY, SOUTHEAST UNIVERSITY, NANJING, CHINA

OBJECTIVES

Polar code is increasing its popularity recently for its capacity-achieving property for B-DMCs. However, when designing decoders for polar code, it has always been an inevitable concern for us to balance the decoding performance and the hardware consumption. The aim of this paper is to:

- 1. combine polar BP decoding and approximate computing together
- 2. propose a hardware efficient polar BP decoder

PRELIMINARIES

For BP decoding, two types of log likelihood ratio (LLR) messages: left-to-right message L and right-to-left message *R*, are involved.

The messages are passed iteratively from left to right and then from right to left according to Eq. (2).

$$\begin{cases} L_{i,j} = f(L_{i+1,2j-1}, g(L_{i+1,2j}, R_{i,j+N/2})), \\ L_{i,j+N/2} = g(f(R_{i,j}, L_{i+1,2j-1}), L_{i+1,2j}), \\ R_{i+1,2j-1} = f(R_{i,j}, g(L_{i+1,2j}, R_{i,j+N/2})), \\ R_{i+1,2j} = g(f(R_{i,j}, L_{i+1,2j-1}), R_{i,j+N/2}); \end{cases}$$
(2)

where

$$f(x,y) = x + y, \tag{3}$$

$$g(x,y) \approx sign(x)sign(y)min(|x|,|y|).$$
 (4)

After the decoding iterations, the *j*-th bit is estimated according to:

$$\hat{u}_j = \begin{cases} 0 & \text{if } R_{1,j} \ge 0, \\ 1 & \text{else.} \end{cases}$$
(5)

REFERENCES

[1] Jin Sha, Xing Liu, Zhongfeng Wang, and Xiaoyang Zeng. A memory efficient belief propagation decoder for polar codes. Communications, China, 12(5):34–41, 2015.

INTRODUCTION

Balancing the decoding performance and hardware implementation complexity has always been an inevitable concern for all designers. However, 100% precision in computation is not always required, especially in some error-resilient systems. In this paper, we combined polar BP decoding and approximate computing together and proposed an efficient approximate BP decoder for polar code. Simulation results show that the proposed approximate BP decoder achieves nearly the same decoding performance as the conventional one with much less hardware cost.

RESULTS



Figure 3: Simulation results of BP decoders with different bits of AOU.

Cost	Original	Proposed	Reduction
ALUT Registers	$97,283 \\ 16214$	$61,958 \\ 14751$	$36.3\% \\ 9.0\%$

Table 1: implementation of different architectures for
 (64 - 32) polar code.

FUTURE RESEARCH

Future works will be directed towards incorporating both scheduling optimization and early termi-

ACHITECTURES

node.

k=2.

The result in Fig. (3) shows that even if when m = 1, the proposed approximate BP decoder still achieves almost the same decoding performance as the conventional one, which makes it possible to remove this AOU in the proposed architecture. In this paper, an approximate BP decoder for polar code is proposed for the first time. Approximate computing schemes are introduced to alleviate the contradiction between higher throughput

nation scheme into our current design.

Figure 1: Proposed approximate architecture for G

For approximate G node, we only compare the high-order n-k bits and the rest k bits are ignored. The detail is shown in Fig. (1) with an example of

The Error Rate (ER) of the proposed approximate G node is considered as follows:

$$ER = \left(\frac{1}{2}\right)^{n-k} \cdot \frac{2^k - 1}{2^{k+1}} = \frac{2^k - 1}{2^{k+1}}.$$
 (1)

According to Eq. (1), for a specific *n*, a larger *k* will

CONCLUSION

and hardware consumption. The flow for designing an approximate polar BP decoder is also proposed. Simulation results show that the proposed approximate computing schemes lead to negligible performance degradation compared with the conventional one, which makes the proposed approximate polar BP decoder highly attractive in the future.

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node.

cause greater performance loss and less hardware consumption. For the proposed approximate architecture, subtraction is directly carried out instead of doing data format conversion before computation. As a result, we only need one data format conversion for F node. $M_a + M_b$ and $M_a - M_b$ are computed at the same time and the magnitude of the final result *s* is chosen from these two values.

Figure 2: Proposed approximate architecture for F

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