Technische Universität München
Institute for Circuit Theory and Signal Processing

Ben-Gurion University of the Negev
Department of Electrical and Computer Engineering

Performance Analysis for Pilot-based 1-bit Channel Estimation with Unknown Quantization Threshold

Manuel Stein[1], Shahar Bar[2], Josef A. Nossek[1], Joseph Tabrikian[2]

[1]Institute for Circuit Theory and Signal Processing, Technische Universität München, Germany
[2]Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Israel
manuel.stein@tum.de, shahba@post.bgu.ac.il, josef.a.nossek@tum.de, joseph@bgu.ac.il

Introduction (I)

Considered Problem:

- Channel parameter estimation with a low-complexity receiver performing 1-bit ADC
- Goal: Characterization of performance loss associated with hard-limiting under an unknown threshold
- Approach: Derivation of performance bounds for parameter estimation with nuisance parameter (offset)

Motivation (II)

Statistical Signal Processing with 1-bit ADC:

- Advantage of 1-bit ADC: simple, cheap and robust analog radio-front end, fast binary DSP
- 1-bit ADC allows high temporal sampling rates → high receive bandwidth
- In practice circuit imperfections and external effects will result in asymmetric 1-bit ADCs

System Model - Ideal and 1-bit System (III)

Receive Signal - Ideal Receiver (∞-bit ADC)

$$\boldsymbol{y} = \zeta \boldsymbol{x} + \boldsymbol{\eta} \quad \text{where} \quad \mathsf{E}_{\boldsymbol{\eta}}\left[\boldsymbol{\eta}\boldsymbol{\eta}^T\right] = \boldsymbol{I}_N$$

Transmit Signal (BPSK, Known Structure)

$$\boldsymbol{x} \in \{-1, 1\}^N \quad \text{with} \quad \frac{1}{N}\sum_{n=1}^{N} x_n = 0$$

Receive Signal - Low-Complexity Receiver (1-bit ADC)

$$\boldsymbol{r} = \operatorname{sign}(\boldsymbol{y} - \alpha \boldsymbol{1}) = \operatorname{sign}(\zeta \boldsymbol{x} + \boldsymbol{\eta} - \alpha \boldsymbol{1})$$

1-bit ADC - Hard-limiter Model

$$[\operatorname{sign}(\boldsymbol{x})]_n = \begin{cases} +1 & \text{if } x_n \geq 0 \\ -1 & \text{if } x_n < 0 \end{cases}, \quad n = 1, \ldots, N$$

Deterministic and Hybrid Approach (IV)

Deterministic - Model Assumptions

$\zeta \rightarrow$ deterministic unknown
$\alpha \rightarrow$ deterministic unknown

Hybrid - Model Assumptions

$\zeta \rightarrow$ random unknown
$\alpha \rightarrow$ deterministic unknown

Deterministic - Estimator (MLE)

$$\hat{\zeta}_{\boldsymbol{y}}(\boldsymbol{y}) \triangleq \arg\max_{\zeta \in \mathbb{R}} p_{\boldsymbol{y}}(\boldsymbol{y}; \zeta)$$

$$\left[\hat{\zeta}_{\boldsymbol{r}}(\boldsymbol{r}) \; \hat{\alpha}_{\boldsymbol{r}}(\boldsymbol{r})\right]^{\mathsf{T}} \triangleq \arg\max_{\zeta, \alpha \in \mathbb{R}} p_{\boldsymbol{r}}(\boldsymbol{r}; \zeta, \alpha)$$

Hybrid - Estimator (MAP / JMAP-MLE)

$$\hat{\zeta}_{\boldsymbol{y}}(\boldsymbol{y}) \triangleq \arg\max_{\zeta \in \mathbb{R}} p_{\boldsymbol{y},\zeta}(\boldsymbol{y}, \zeta)$$

$$\left[\hat{\zeta}_{\boldsymbol{r}}(\boldsymbol{r}) \; \hat{\alpha}_{\boldsymbol{r}}(\boldsymbol{r})\right]^{\mathsf{T}} \triangleq \arg\max_{\zeta, \alpha \in \mathbb{R}} p_{\boldsymbol{r},\zeta}(\boldsymbol{r}, \zeta; \alpha)$$

Deterministic - Performance (MSE)

$$\text{MSE}_{\boldsymbol{y}}(\zeta) \triangleq \mathsf{E}_{\boldsymbol{y};\zeta}\left[\left(\hat{\zeta}_{\boldsymbol{y}}(\boldsymbol{y}) - \zeta\right)^2\right]$$

$$\text{MSE}_{\boldsymbol{r}}(\zeta, \alpha) \triangleq \mathsf{E}_{\boldsymbol{r};\zeta,\alpha}\left[\left(\hat{\zeta}_{\boldsymbol{r}}(\boldsymbol{r}) - \zeta\right)^2\right]$$

Hybrid - Performance (MSE)

$$\text{MSE}_{\boldsymbol{y}} \triangleq \mathsf{E}_{\boldsymbol{y},\zeta}\left[\left(\hat{\zeta}_{\boldsymbol{y}}(\boldsymbol{y}) - \zeta\right)^2\right]$$

$$\text{MSE}_{\boldsymbol{r}}(\alpha) \triangleq \mathsf{E}_{\boldsymbol{r},\zeta;\alpha}\left[\left(\hat{\zeta}_{\boldsymbol{r}}(\boldsymbol{r}) - \zeta\right)^2\right]$$

Deterministic Approach - Hard-limiting Loss (V)

Cramér-Rao Lower Bound - Ideal System with ∞-bit ADC

$$\text{MSE}_{\boldsymbol{y}}(\zeta) \stackrel{\text{a}}{=} F_y^{-1}(\zeta) = \frac{1}{N}$$

Cramér-Rao Lower Bound - Low-Complexity System with 1-bit ADC

$$\text{MSE}^{\star}_{\boldsymbol{r}}(\zeta, \alpha) \stackrel{\text{a}}{=} F^{-1}_{r,\zeta\zeta}(\zeta, \alpha)$$

$$\text{MSE}_{\boldsymbol{r}}(\zeta, \alpha) \stackrel{\text{a}}{=} \frac{F_{r,\alpha\alpha}(\zeta, \alpha)}{F_{r,\zeta\zeta}(\zeta, \alpha) F_{r,\alpha\alpha}(\zeta, \alpha) - F^2_{r,\zeta\alpha}(\zeta, \alpha)}$$

$$F_{r,\zeta\zeta}(\zeta, \alpha) = \mathsf{E}_{\boldsymbol{r};\zeta,\alpha}\left[\left(\frac{\partial \ln p_{\boldsymbol{r}}(\boldsymbol{r}; \zeta, \alpha)}{\partial \zeta}\right)^2\right] = \frac{N}{2}\left(\phi_+(\zeta, \alpha) + \phi_-(\zeta, \alpha)\right)$$

$$F_{r,\alpha\alpha}(\zeta, \alpha) = \mathsf{E}_{\boldsymbol{r};\zeta,\alpha}\left[\left(\frac{\partial \ln p_{\boldsymbol{r}}(\boldsymbol{r}; \zeta, \alpha)}{\partial \alpha}\right)^2\right] = \frac{N}{2}\left(\phi_+(\zeta, \alpha) + \phi_-(\zeta, \alpha)\right)$$

$$F_{r,\zeta\alpha}(\zeta, \alpha) = \mathsf{E}_{\boldsymbol{r};\zeta,\alpha}\left[\frac{\partial \ln p_{\boldsymbol{r}}(\boldsymbol{r}; \zeta, \alpha)}{\partial \zeta}\frac{\partial \ln p_{\boldsymbol{r}}(\boldsymbol{r}; \zeta, \alpha)}{\partial \alpha}\right] = \frac{N}{2}\left(\phi_+(\zeta, \alpha) - \phi_-(\zeta, \alpha)\right)$$

$$\phi_{\pm}(\zeta, \alpha) \triangleq \frac{\exp\left(-(\alpha \pm \zeta)^2\right)}{2\pi\left(\mathrm{Q}(\alpha \pm \zeta) - \mathrm{Q}^2(\alpha \pm \zeta)\right)}$$

Hard-limiting Loss for the Deterministic Approach

$$\chi(\zeta, \alpha) \triangleq \frac{\text{MSE}_{\boldsymbol{y}}(\zeta)}{\text{MSE}_{\boldsymbol{r}}(\zeta, \alpha)} = 2\frac{\phi_+(\zeta, \alpha)\phi_-(\zeta, \alpha)}{\phi_+(\zeta, \alpha) + \phi_-(\zeta, \alpha)}$$

$$\chi^{\star}(\zeta, \alpha) \triangleq \frac{\text{MSE}_{\boldsymbol{y}}(\zeta)}{\text{MSE}^{\star}_{\boldsymbol{r}}(\zeta, \alpha)} = \frac{1}{2}\left(\phi_+(\zeta, \alpha) + \phi_-(\zeta, \alpha)\right)$$

Hybrid Approach - Hard-limiting Loss (VI)

Expected Cramér-Rao Lower Bound - Ideal System with ∞-bit ADC

$$\text{MSE}_{\boldsymbol{y}} \stackrel{\text{a}}{=} \mathsf{E}_{\zeta}\left[F_y^{-1}(\zeta)\right] = \frac{1}{N}$$

Expected Cramér-Rao Lower Bound - Low-Complexity System with 1-bit ADC

$$\text{MSE}^{\star}_{\boldsymbol{r}}(\alpha) \stackrel{\text{a}}{=} \mathsf{E}_{\zeta}\left[F^{-1}_{r,\zeta\zeta}(\zeta, \alpha)\right]$$

$$\begin{aligned}\text{MSE}_{\boldsymbol{r}}(\alpha) &\stackrel{\text{a}}{=} \mathsf{E}_{\zeta}\left[\frac{F_{r,\alpha\alpha}(\zeta, \alpha)}{F_{r,\zeta\zeta}(\zeta, \alpha) F_{r,\alpha\alpha}(\zeta, \alpha) - F^2_{r,\zeta\alpha}(\zeta, \alpha)}\right] \\ &= \mathsf{E}_{\zeta}\left[\frac{\frac{2}{N}\left(\phi_+(\zeta, \alpha) + \phi_-(\zeta, \alpha)\right)}{\left(\phi_+(\zeta, \alpha) + \phi_-(\zeta, \alpha)\right)^2 - \left(\phi_+(\zeta, \alpha) - \phi_-(\zeta, \alpha)\right)^2}\right] \\ &= \frac{1}{2N}\left(\mathsf{E}_{\zeta}\left[\frac{1}{\phi_-(\zeta, \alpha)}\right] + \mathsf{E}_{\zeta}\left[\frac{1}{\phi_+(\zeta, \alpha)}\right]\right) \\ &= \frac{1}{N}\Psi_H\end{aligned}$$

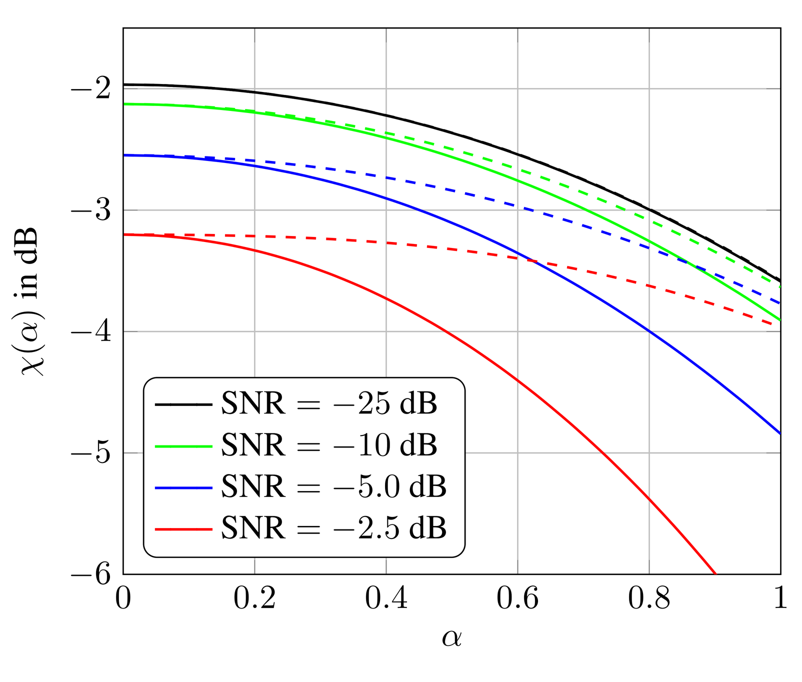
$$\Psi_H \triangleq \mathsf{E}_{\zeta}\left[\frac{1}{\phi_-(\zeta, \alpha)}\right] = \mathsf{E}_{\zeta}\left[\frac{1}{\phi_+(\zeta, \alpha)}\right]$$

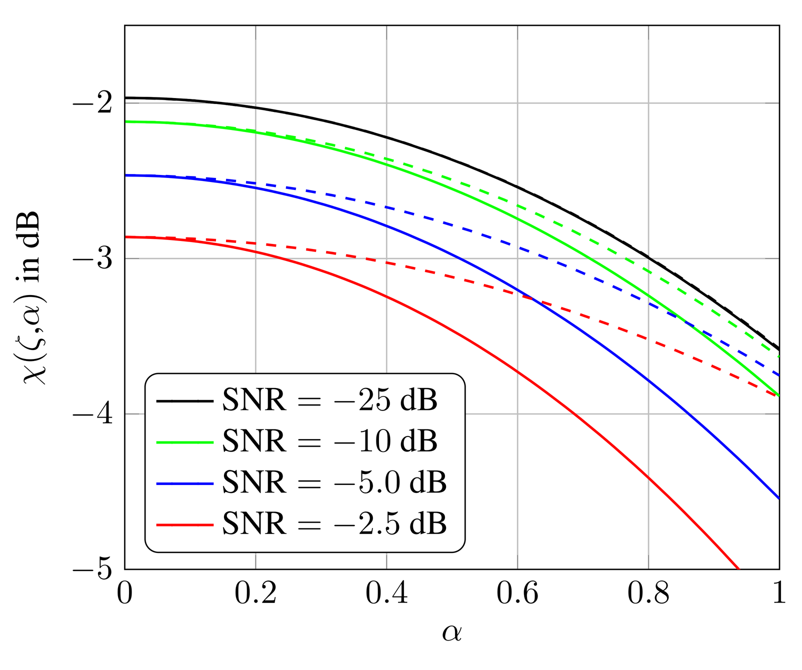
Hard-limiting Loss for the Hybrid Approach

$$\chi(\alpha) \triangleq \frac{\text{MSE}_{\boldsymbol{y}}}{\text{MSE}_{\boldsymbol{r}}(\alpha)} \stackrel{\text{a}}{=} \Psi_H^{-1}$$

$$\chi^{\star}(\alpha) \triangleq \frac{\text{MSE}_{\boldsymbol{y}}}{\text{MSE}^{\star}_{\boldsymbol{r}}(\alpha)} \stackrel{\text{a}}{=} \frac{1}{2\,\mathsf{E}_{\zeta}\left[\frac{1}{\phi_+(\zeta, \alpha) + \phi_-(\zeta, \alpha)}\right]}$$

Performance Analysis - Results (VII)





Summary and Insights (VIII)

- Characterization of channel parameter estimation performance under 1-bit ADC with unknown threshold
- Analysis of two different estimation approaches (deterministic/hybrid)
- Performance analysis through performance bounds for MLE and MAP/JMAP-ML
- Low SNR regime: additional performance loss (offset estimation) vanishes
- Medium SNR: loss vanishes for small offset values (requires careful 1-bit ADC hardware design)

Further Work (IX)

- Analytic characterization of the performance loss in the low SNR regime
- Advanced channel estimation problems (e.g. ISI wireless channel)