Hardware Implementation of FIR/IIR Digital Filters Using Integral Stochastic Computation

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March 25, 2016

2016 IEEE International Conference on
Acoustics, Speech and Signal Processing

Outline

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- Stochastic Computing (SC)
- Previously Proposed Filters Based on SC
- Integral Stochastic Computing (ISC)
- The Proposed FIR/IIR Filters Based on ISC
- Simulation and Implementation Results
- Conclusion

Introduction

- Stochastic Computing (SC) Provides some advantages over binary radix implementation:
  - Low-cost VLSI implementation
  - Fault tolerant hardware
- Despite its advantages, it introduces some challenges:
  - High processing time
  - Low accuracy
- Therefore, SC was viewed as not suitable for applications which require high accuracy such as digital filters.

Stochastic Representation

- In SC, a real value $x \in [0, 1]$ is represented as a sequence of random bits, $X_i \in \{0, 1\}$, $i \in \{1, 2, \ldots, N\}$, where N denotes the stream length. The number x corresponds to the expected value of an element of the sequence:

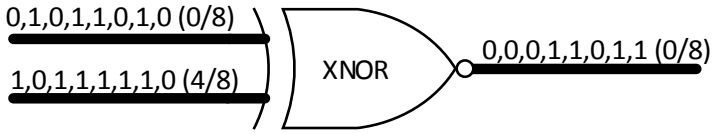
$$E[X_i] = x$$

- This stochastic representation is known as the *unipolar* format. The *bipolar* format is also used for stochastic representation of a real number $x \in [-1, 1]$ by setting:

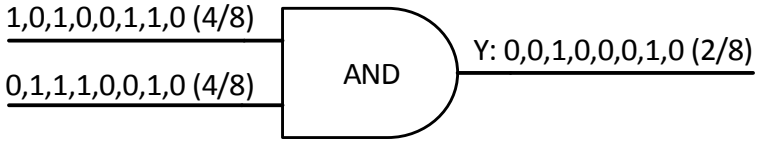
$$E[X_i] = (x + 1)/2$$

Computational Elements in SC

- Multiplication:

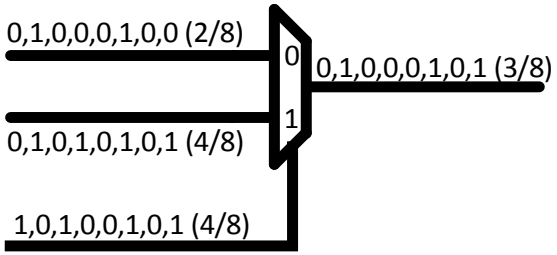


Bipolar Multiplier



Unipolar Multiplier

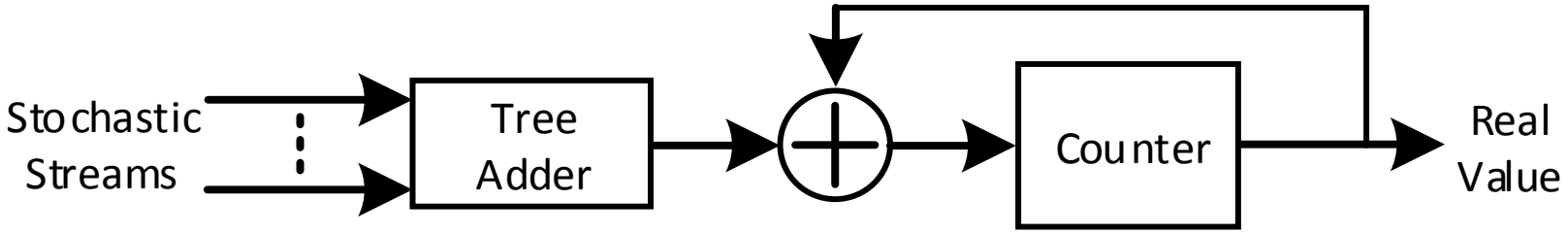
- Addition:



Scaled Adder

Accumulative Parallel Counter (APC)

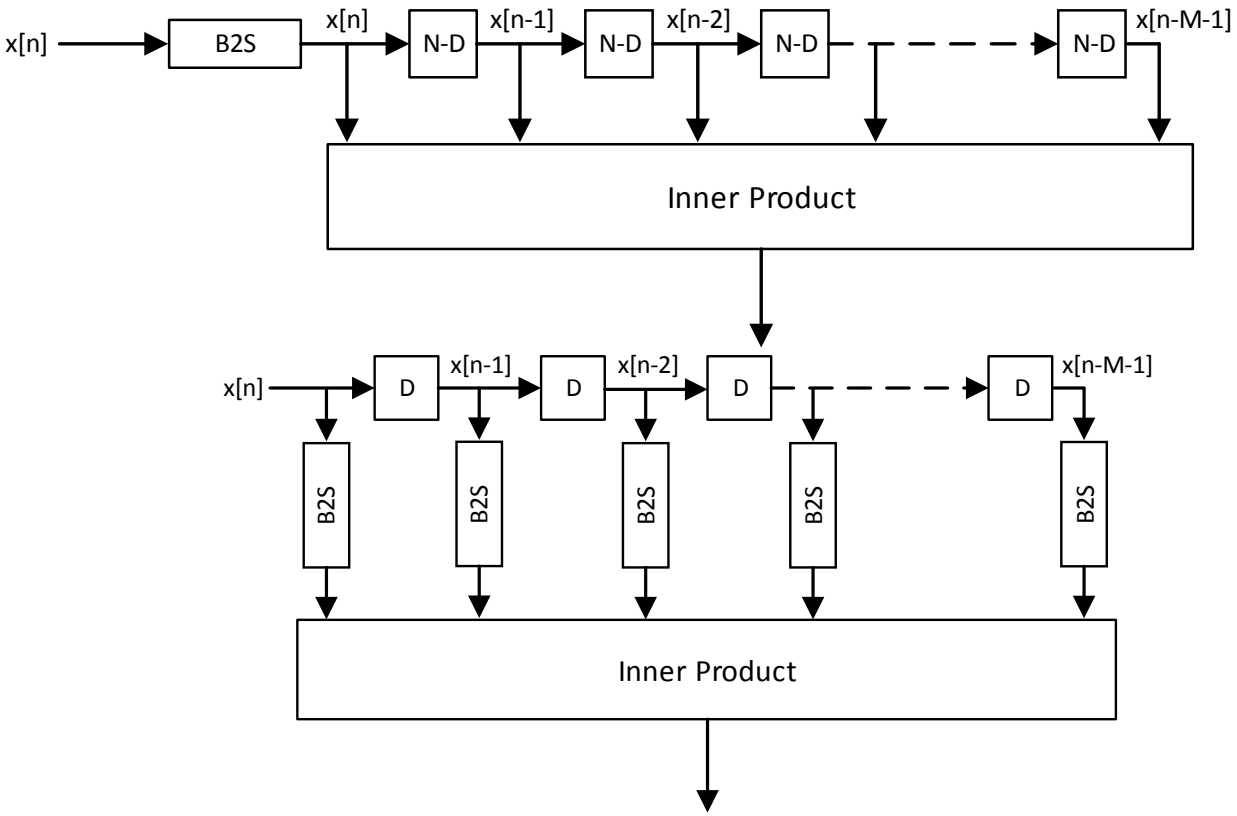
- It was introduced in [1]
- The APC uses a binary tree-adder to perform additions
- The output of APC is in binary radix domain
- The APC is restricted to the applications requiring information in binary domain after additions



[1] Pai-Shun Ting and J.P. Hayes, "Stochastic Logic Realization of Matrix Operations," in 2014 17th Euromicro Conference on Digital System Design (DSD), Aug 2014, pp. 356–364.

Previously Proposed FIR Filter Based on SC

Two conventional approaches used for stochastic implementation of FIR filters by delaying (a) the stochastic sequence and (b) the binary numbers [2].



[2] Yun-Nan Chang and K.K. Parhi, "Architectures for digital filters using stochastic computing," in Proc. 2013 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), May 2013, pp. 2697–2701.

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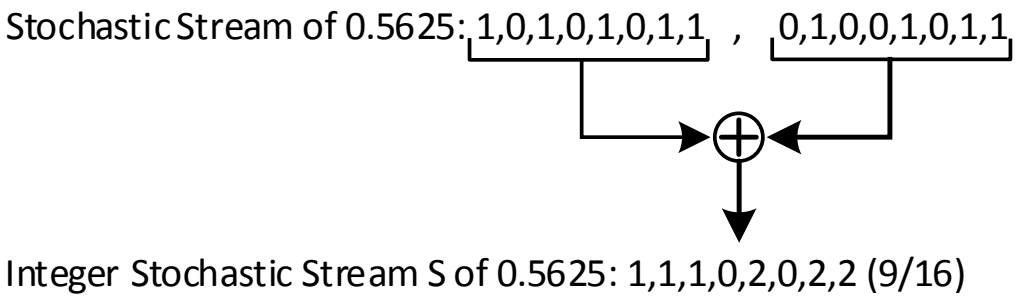
Integral Stochastic Computing

- Integral SC was introduced in [3]
- Each element S_i of the integer stochastic stream represents a real value s ∈ [0, m]
- ISC can be generated by summing up m binary stochastic streams as follows:

$$S_i = \sum_{j=1}^{m} X_i^j$$

- where X_i^j denotes an element of stochastic stream X^j representing the real value x^j ∈ [0, 1].
- Then, the expected value of the sequence element S_i is given by:

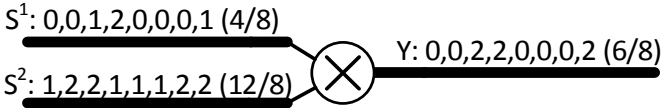
$$s = \mathrm{E}[S_i] = \sum_{j=1}^{m} x^j$$



[3] A. Ardakani, F. Leduc-Primeau, N. Onizawa, T. Hanyu and W. J. Gross, "VLSI Implementation of Deep Neural Network Using Integral Stochastic Computing," CoRR, vol. abs/1509.08972, 2015. [Online]. Available: http://arxiv.org/abs/1509.08972.

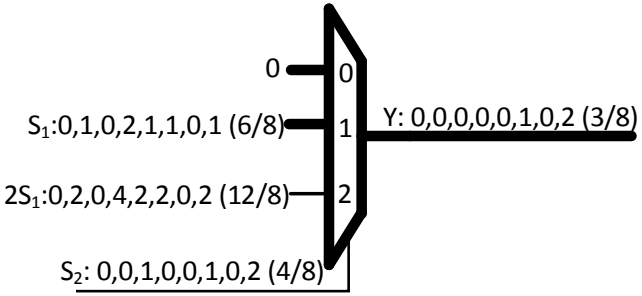
ISC Computational Elements

- It was shown that additions are performed by using binary adders, and multiplications can be performed by binary multipliers.

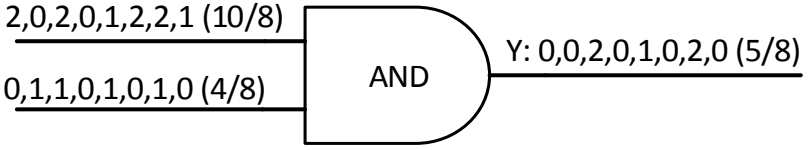


- Solutions to compensate the complexity of ISC multiplier:

Coefficient values mostly lie in [-2, 2] and multiplications are then performed using a multiplexer as follows:

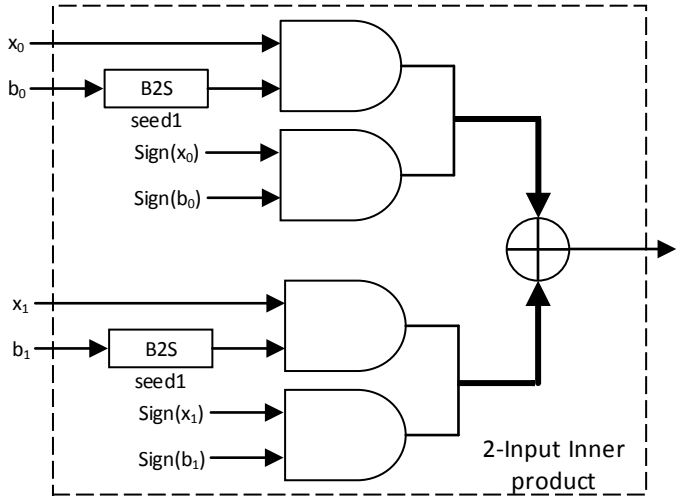


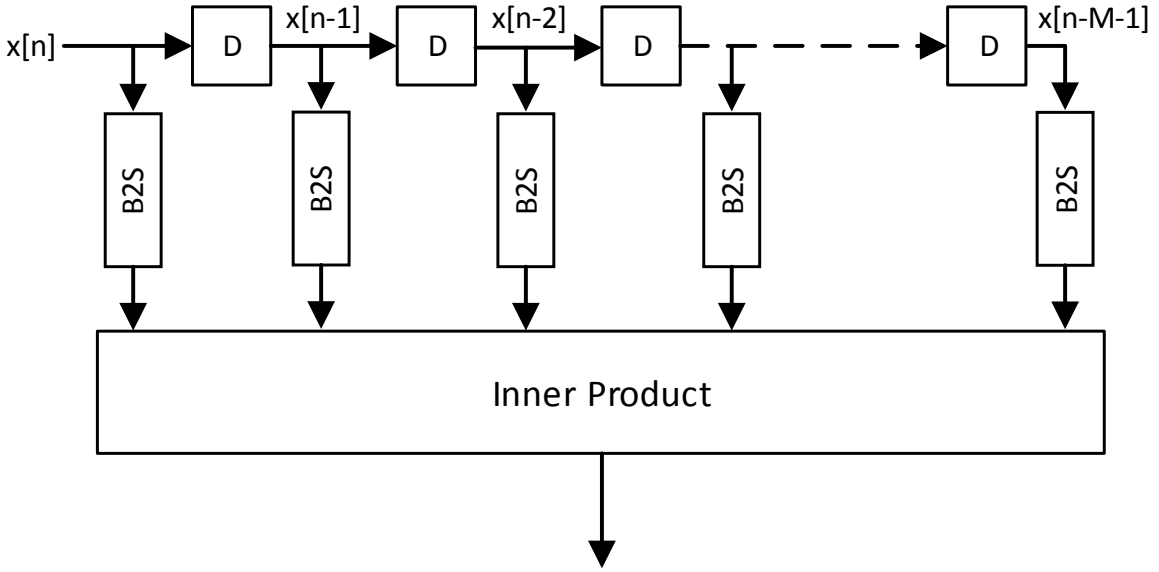
If one of the inputs is in SC format, multiplication can be performed using bit-wise AND gate



The proposed FIR Filter

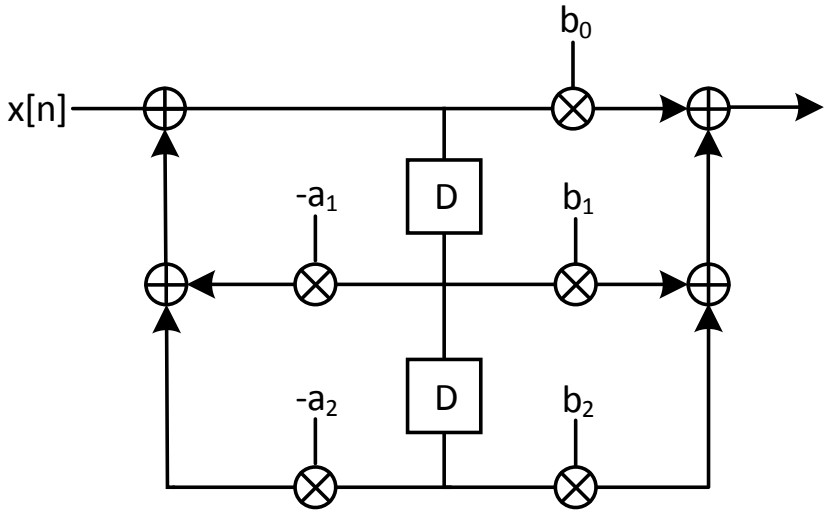
- Due to uncorrelated ISC addition, the proposed FIR filter only requires two LFSR units to perform computations as opposed to conventional stochastic filters



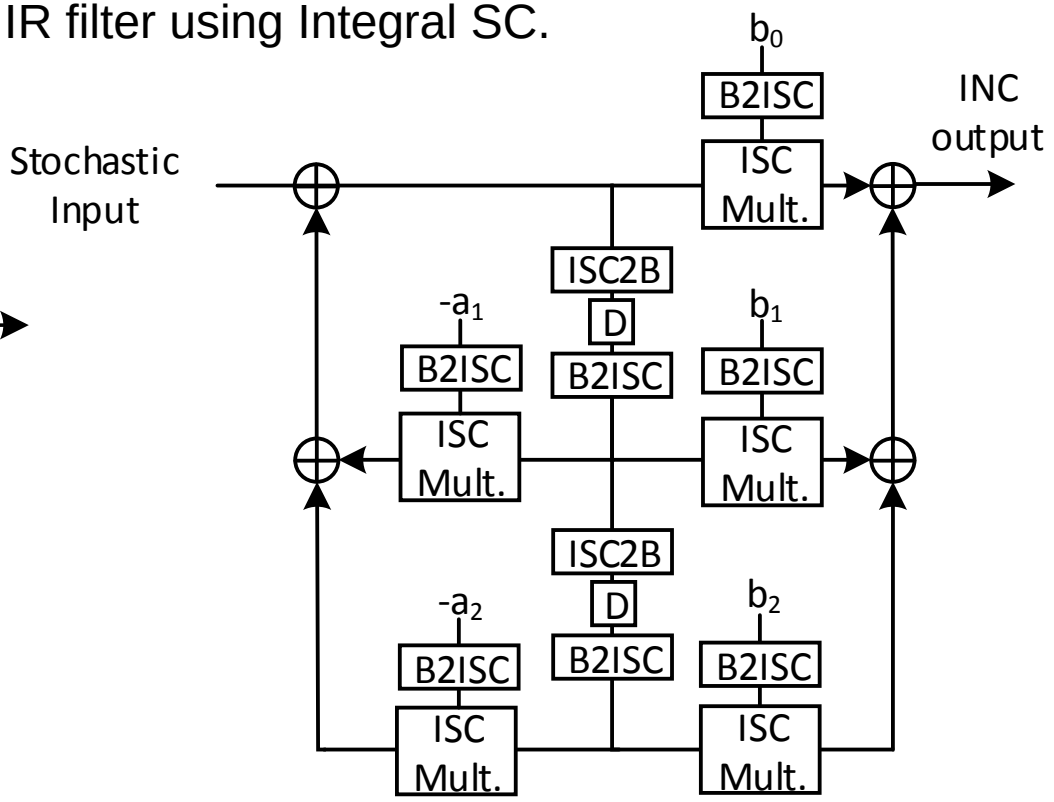


The Proposed IIR Filter Based on ISC

- High-order filter can be achieved by cascading the proposed stochastic architecture of a second-order IIR filter using Integral SC.



The direct-form II structure for a second-order IIR filter.



The proposed stochastic architecture of a second-order IIR filter using Integral SC.

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FIR Filter Simulation Results

The output error-to-signal power ratio of the proposed stochastic FIR filters

Filter Order	**Low-pass Cut-off Frequency**			
	0.2π	0.4π	0.6π	0.8π
45	0.0014	0.0012	2.9×10^{-4}	5.3×10^{-4}
55	0.0012	0.0014	4.28×10^{-4}	5.3×10^{-4}
Filter Order	**High-pass Cut-off Frequency**			
	0.2π	0.4π	0.6π	0.8π
46	0.0012	0.0011	0.0012	0.0021
56	2.8×10^{-4}	8.1×10^{-4}	0.0011	0.0018

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IIR Filter Simulation Results

The output error-to-signal power ratio of the proposed stochastic IIR filters

Filter Type	Direct Form [2]	Proposed
Low-Pass	42.5721	0.0030
High-Pass	43.3597	0.0011

[2] Yun-Nan Chang and K.K. Parhi, "Architectures for digital filters using stochastic computing," in Proc. 2013 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), May 2013, pp. 2697–2701.

Hardware Implementation Results

The hardware implementation in a 65 nm CMOS technology @ 400 MHz for a stream length of L.

Filter Type	**FIR**		**IIR**	
Implementation Type	ISC	Binary	ISC	Binary
Filter Order	56	56	6	6
Area (µm)	22,526	218,905	7,620	36,921
Latency (ns)	2.5 × L	2.5	2.5 × L	2.5

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Conclusion

- The proposed FIR filter uses the APC and AND gate as its main computational units to perform the additions and multiplications.
- The error rate of the proposed FIR architecture remains constant as the filter order increases.
- A second-order direct-form II structure of an IIR filter is proposed using the Integral SC.
- A high-order IIR filter can be obtained by cascading series of second-order direct-form II structures.
- The error-to-signal power ratio results of the proposed IIR filter showed a roughly 4 orders of magnitude improvement compared to the conventional structure.

Thank you!