

Massive MIMO Processing at the Semiconductor Edge: Exploring the System and Circuit Margins for Power Saving

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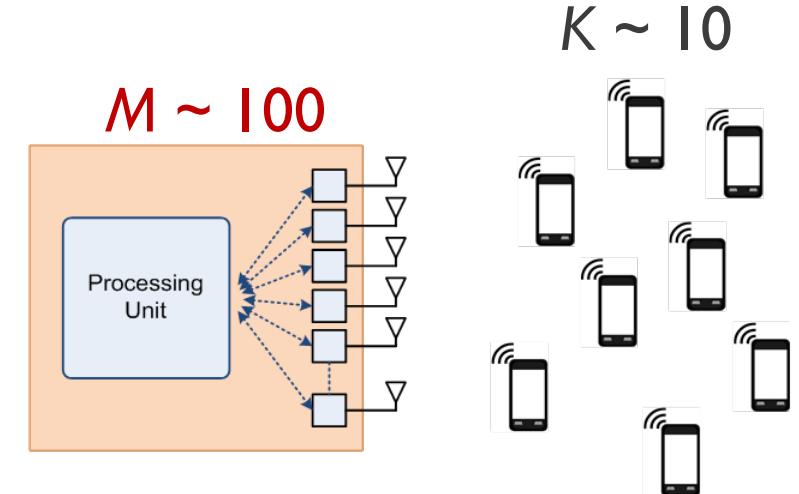
Why Massive MIMO?

5G needs: more capacity/Watt/\$

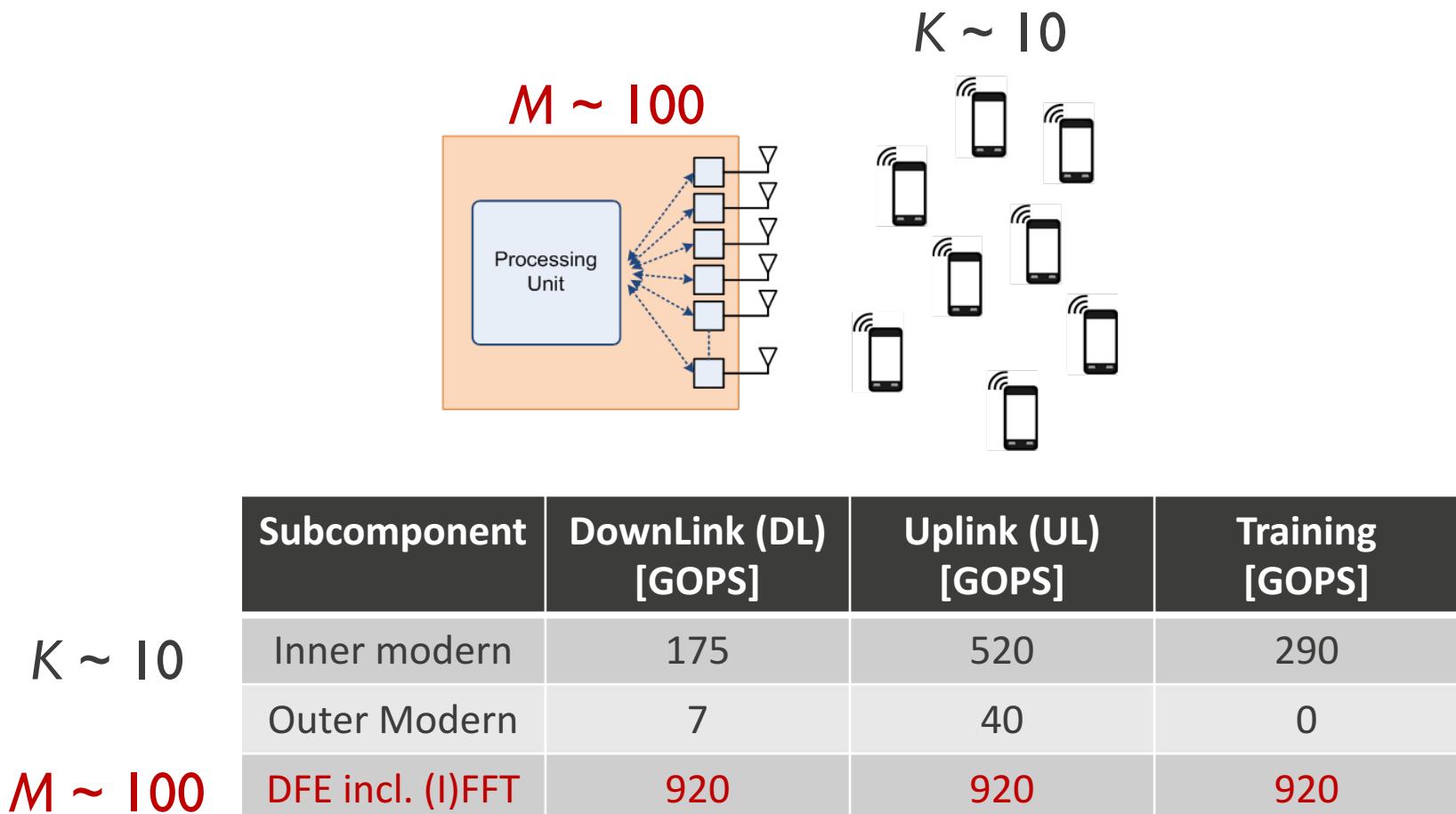
- Millimeter waves
- Heterogeneous networks
- **Massive MIMO**

Key features:

- M (base station antennas) $\gg K$ (users) $\gg 1$
- MU-MIMO precoding (DL) or linear detection (UL)
- Uplink-based Channel-State Information
- **Low-cost low-power low-accuracy hardware (per-antenna)**

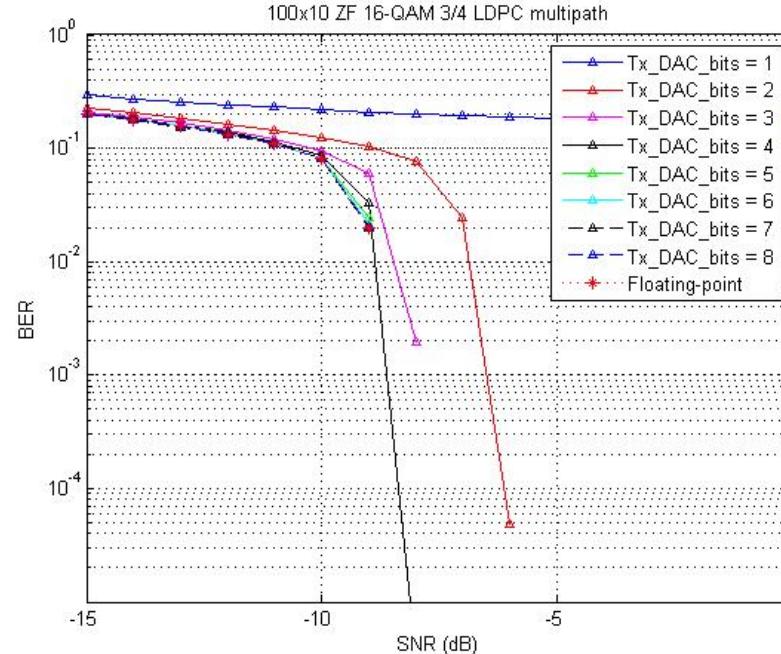


Is massive processing an issue?



BS (Base station) complexity of digital components for 100x10 Massive MIMO, with 20 MHz bandwidth, 3 bps/Hz (16-QAM, coding rate 3/4)

Embracing low accuracy hardware (per-antenna) low-quantization

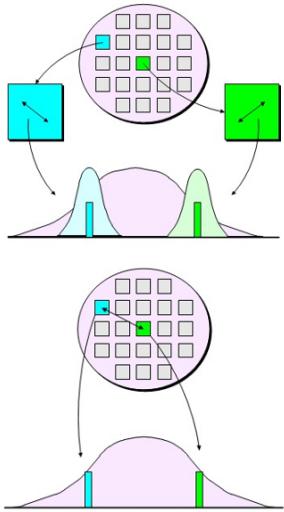


C. Dessel, EuCNC, Validation of low-accuracy ...

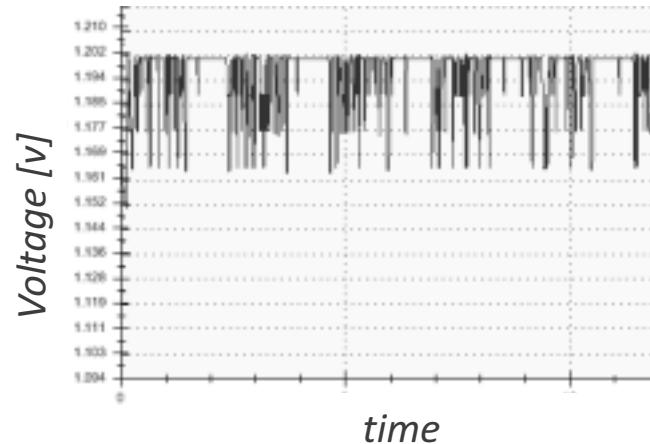
3-bit DAC for 16-QAM

It embraces noisy signal processing

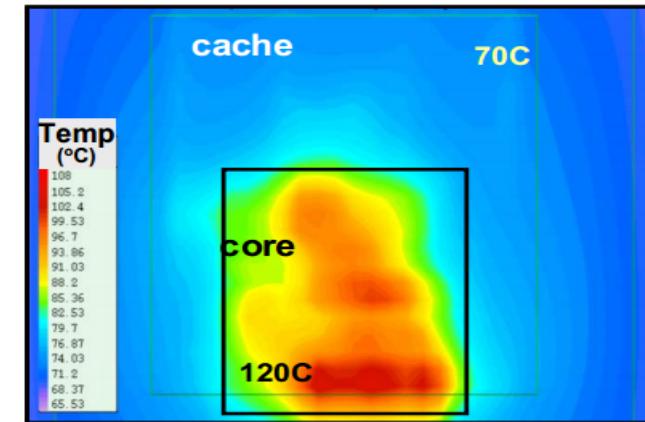
Semiconductors suffer from variations



Process Variations

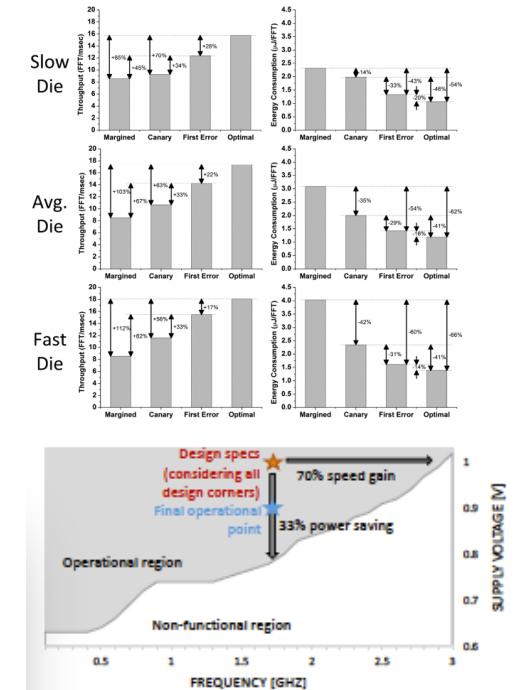
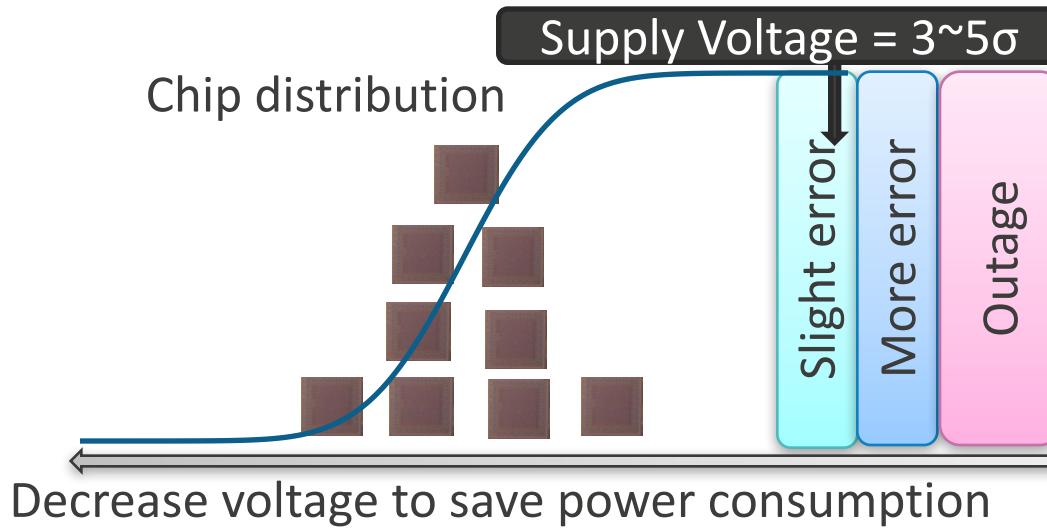


Voltage fluctuation



Temperature variation

Chips sacrifice power & cost to provide correctness

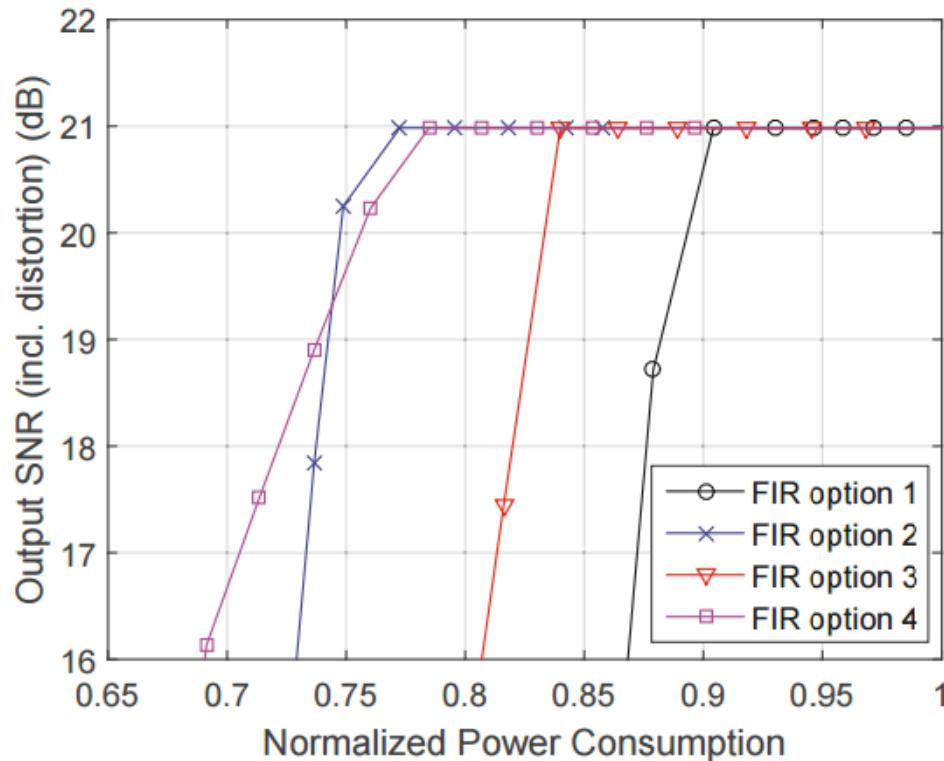


~40% power wasted to guarantee correctness

Refs

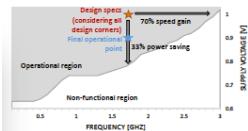
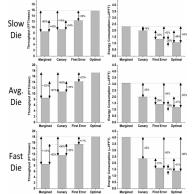
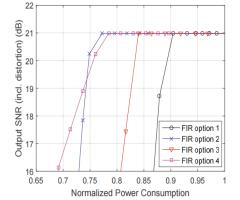
Ref: 54% from 45nm M. Fojtik, JSSC13, Bubble Razor ...: Fig.12 Energy Slow die and avg. Die, first error power saving 33% from 28nm Y. Huang, ASSCC16, a 28nm ... : Fig. 7(b)

What if processing at the CMOS edge? 'Only' quality degradation



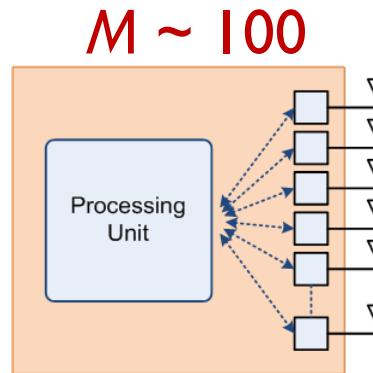
65nm, Y. Liu, TVLSI10, Computation error ...

Processing Massive MIMO at CMOS edge



$$SDDR = 10 \log \frac{\sigma_s^2}{\sigma_d^2}$$

Signal-to-Digital-Distortion

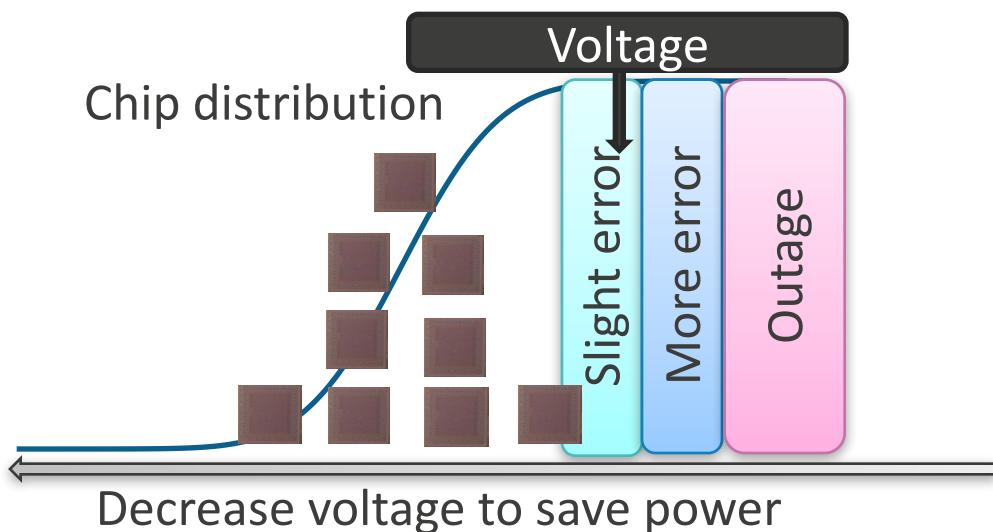


$K \sim 10$

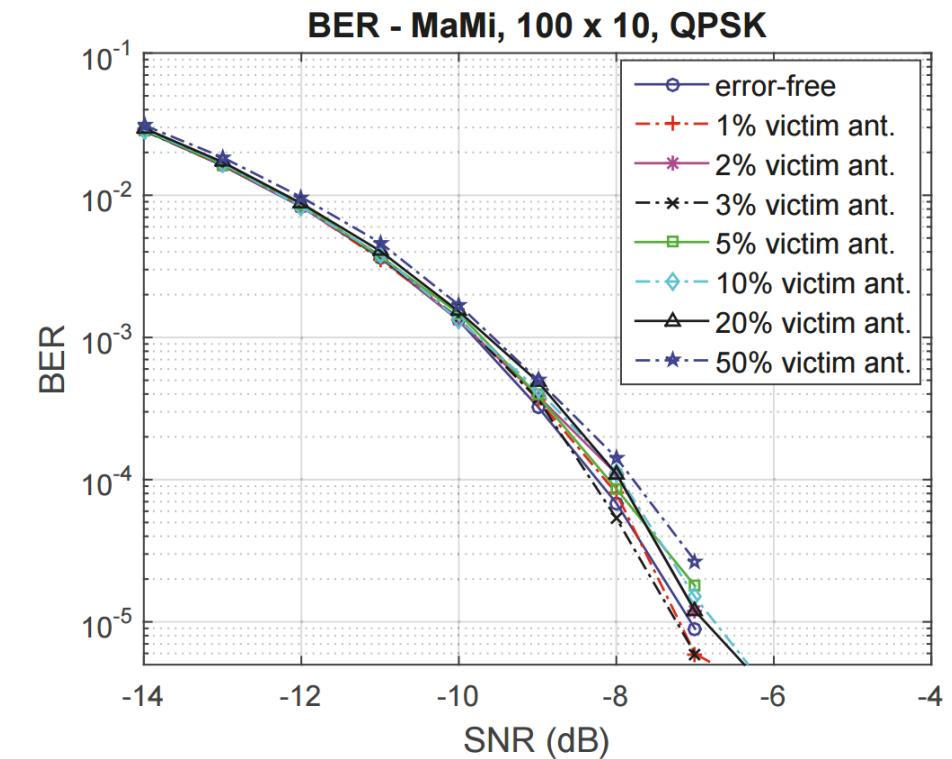


Massive MIMO, 100x10, DownLink, TDD, LTE-like

Only slight degradation when embracing slight digital distortion error

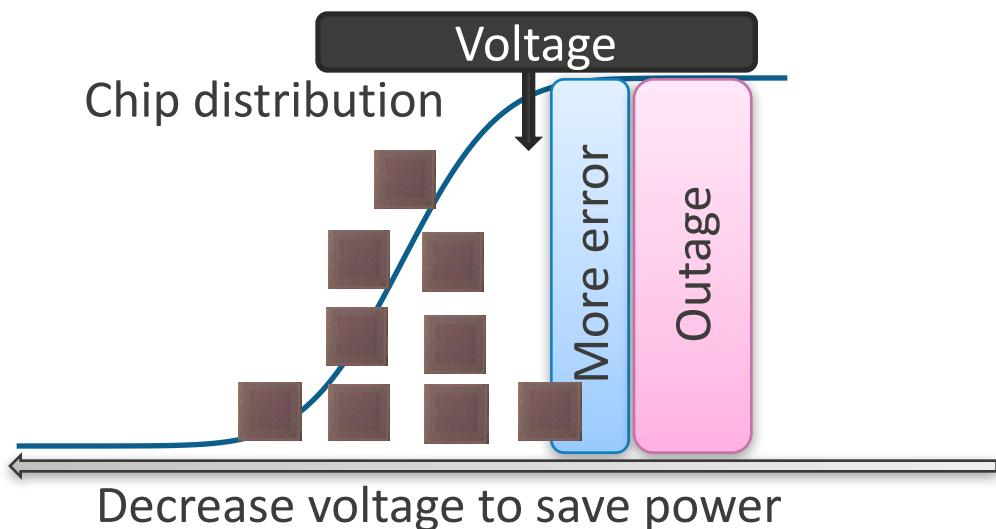


When Voltage decreases, more antennas facing slight error, or even outage

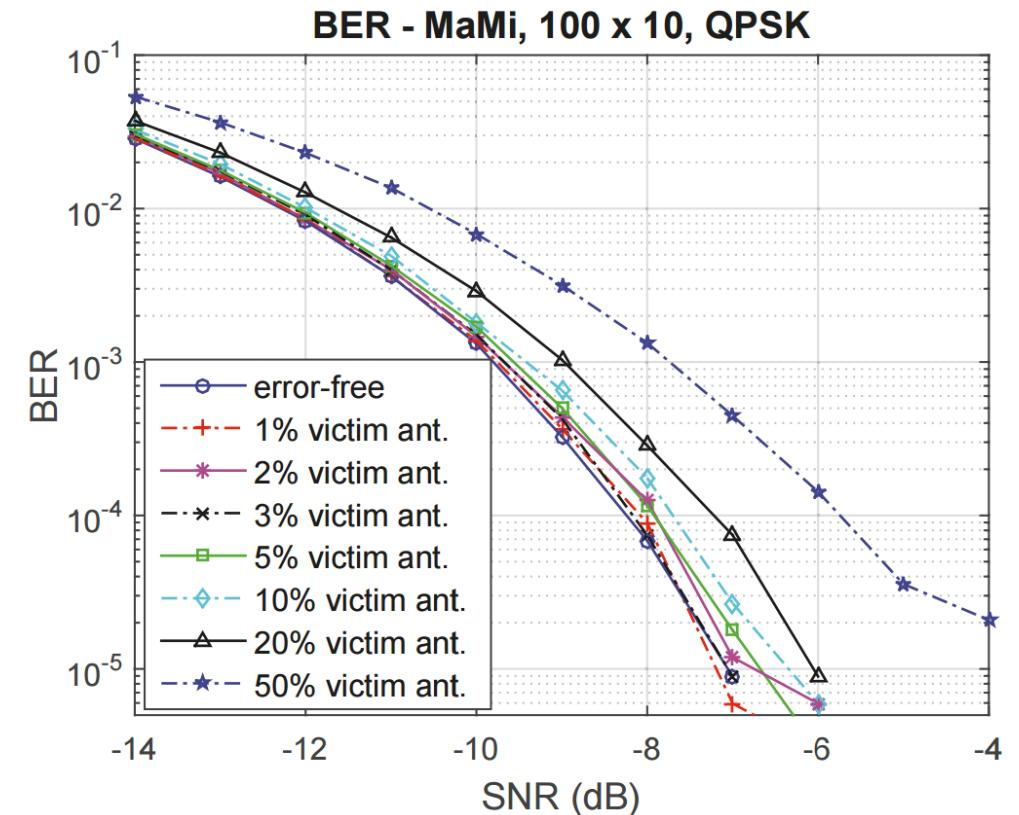


*Slight error,
Signal-to-Digital Distortion Ratio = 10dB*

Acceptable degradation even with heavy distortion

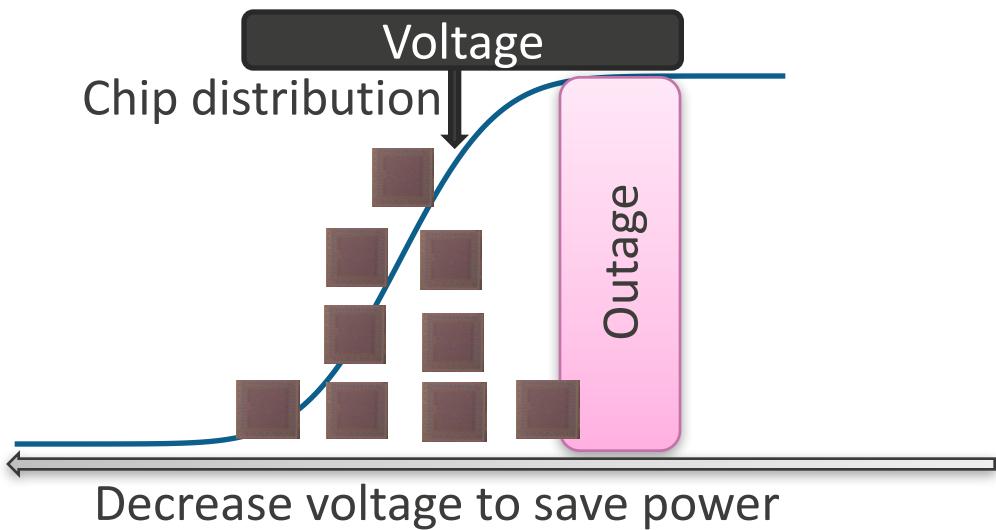


When Voltage decreases, more antennas facing more errors



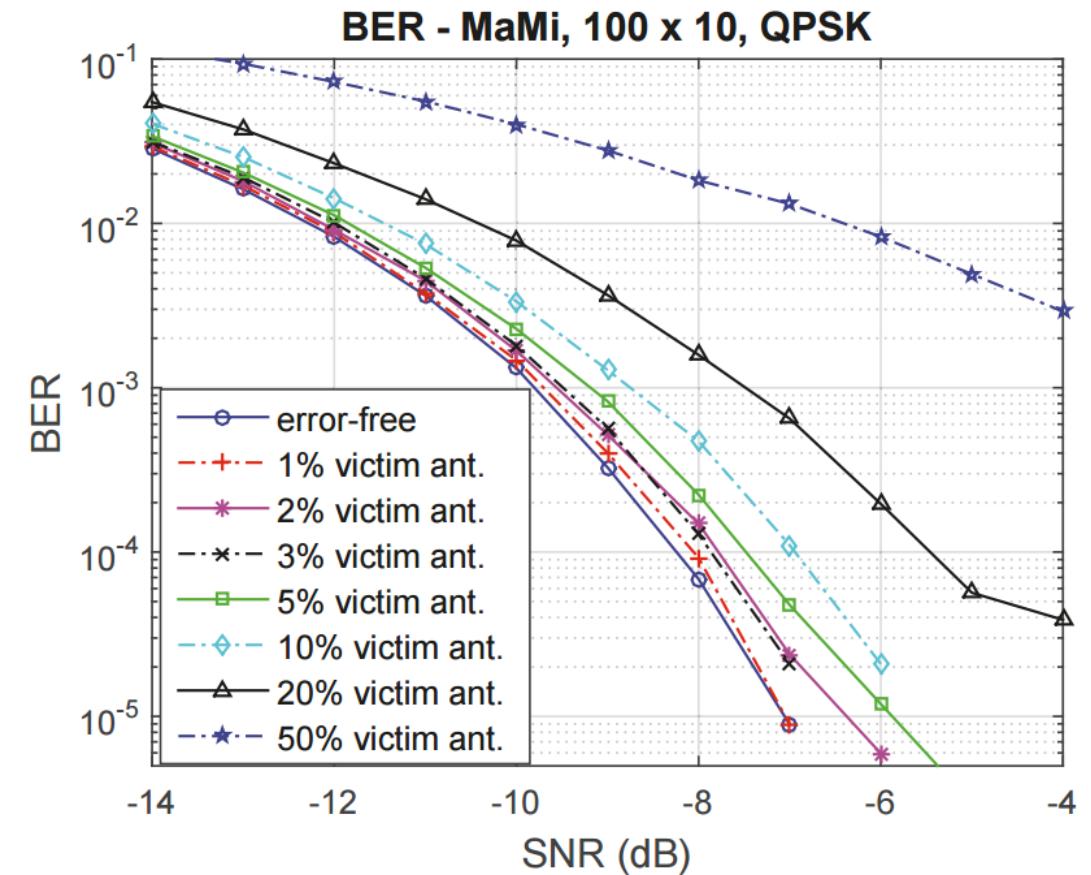
*Extensive error,
Signal-to-Digital Distortion Ratio = 0 dB*

Manageable even with completely outage



When Voltage decreases, antenna outage occurs

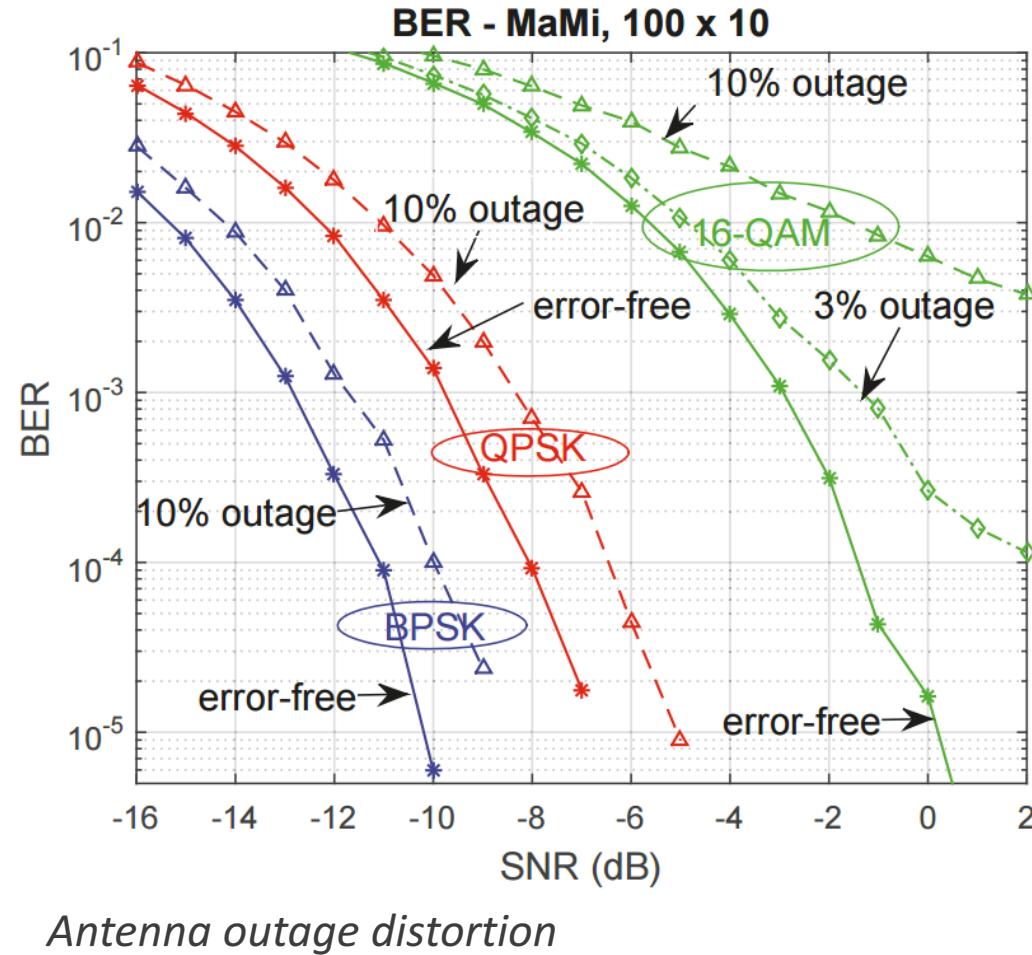
It tolerate 10% outage, (1.3 σ variability margin),
43%~54% power saving [ref]



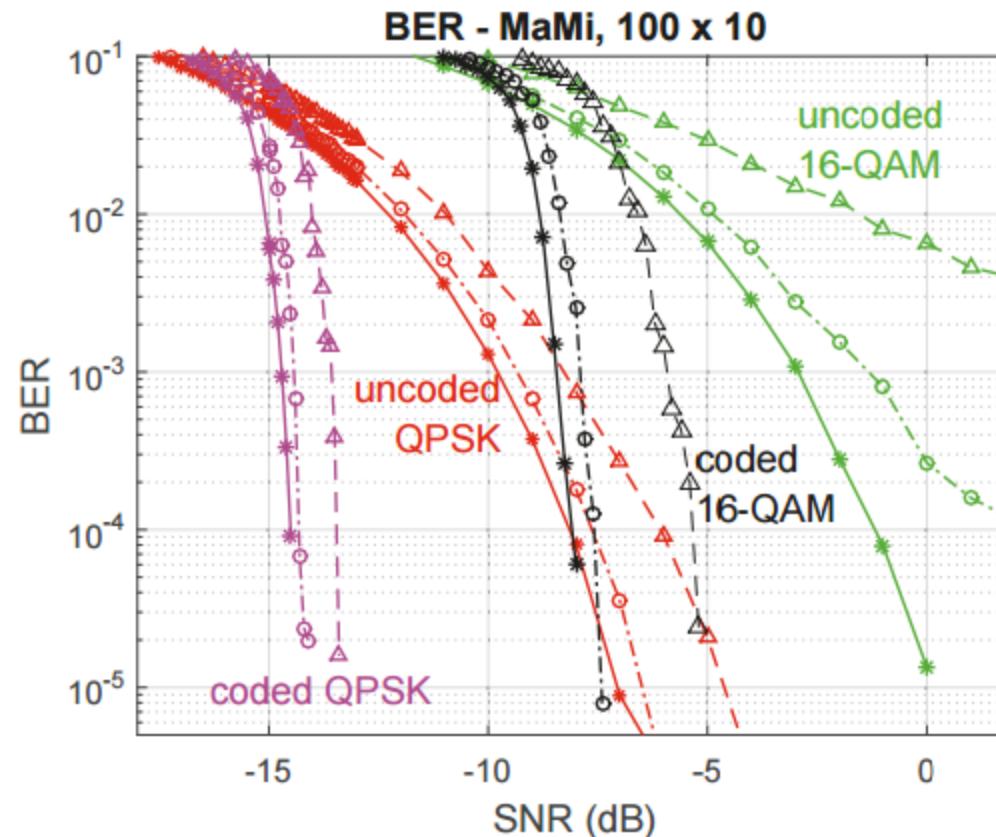
Antenna completely outage,
output stuck at a fixed value

[Ref] M. Fojtik, JSSC13, Bubble Razor ...: Fig.12 Energy Slow die and avg. Die, first error power saving

Simpler modulations are more robust to embrace distortions



On error-coded performance SNR degradation is even smaller

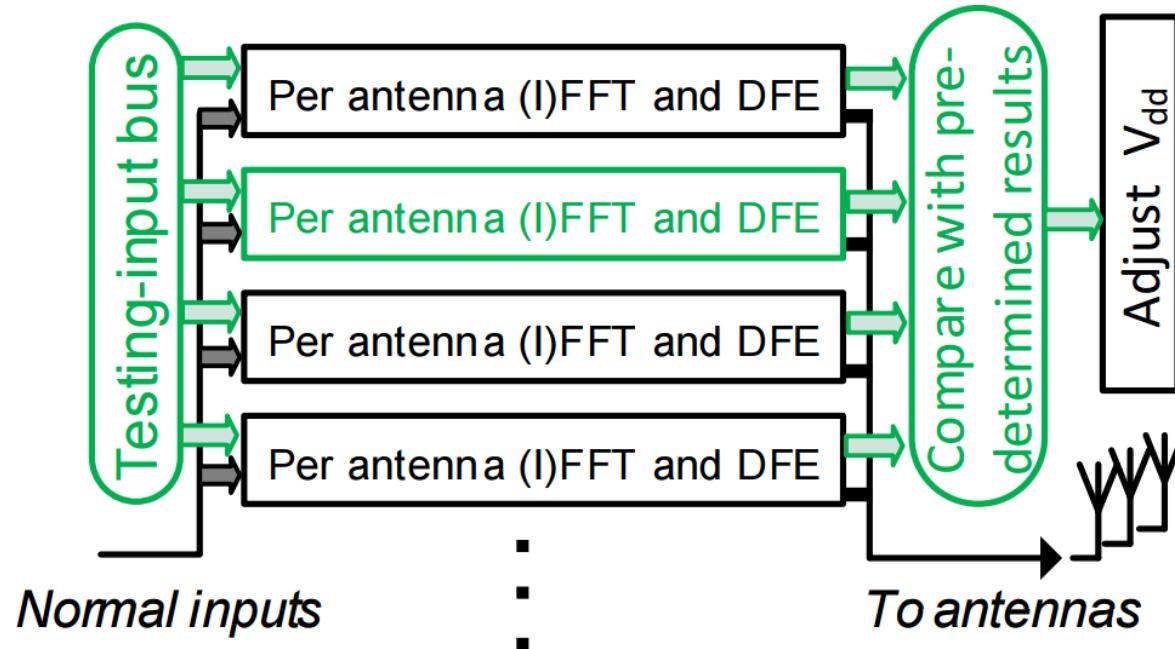


Antenna outage distortion ($\frac{3}{4}$ LDPC coding)

Leftmost error-free, middle 3% victim, right 10% victim

Solutions to harness variation (error)

Monitor variation on-the-fly



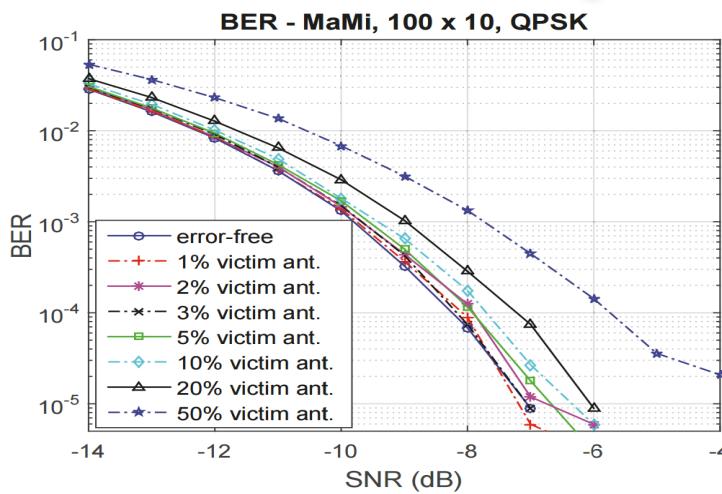
Monitor per-antenna functionality, to decide whether to adjust environment (V_{dd}), continue, or discard antenna ...

Case study:

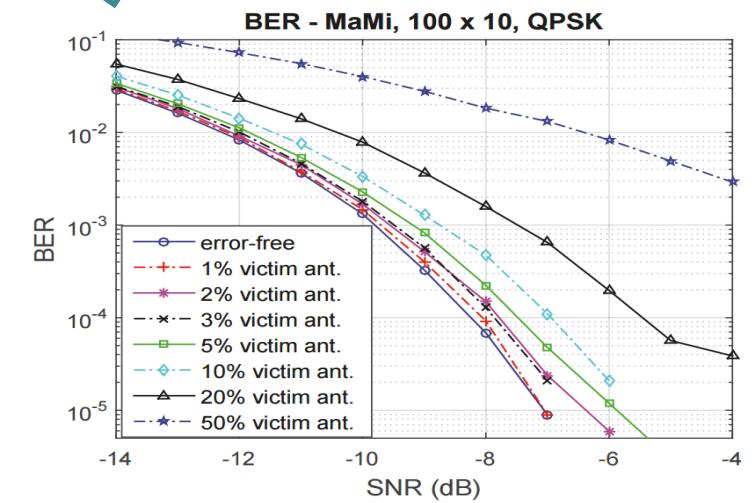
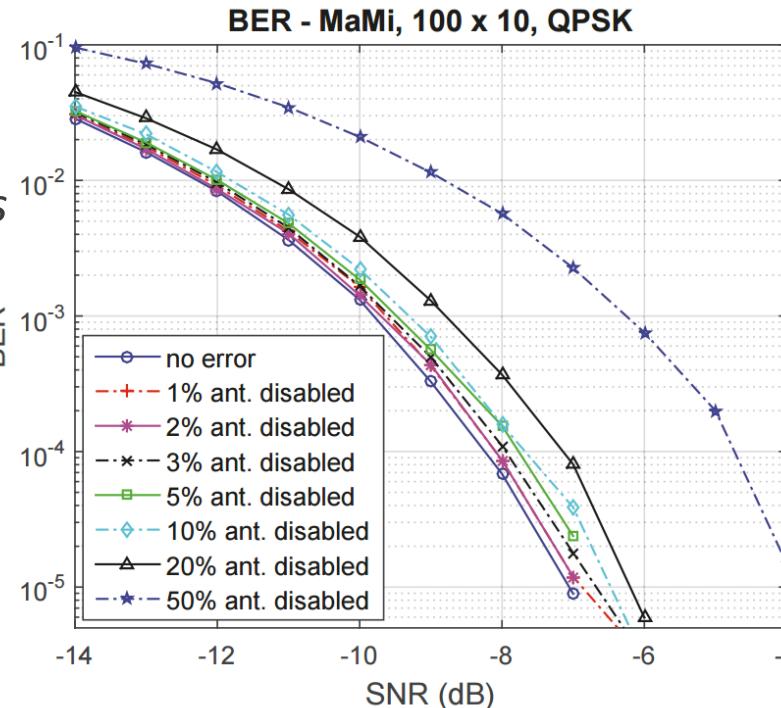
When facing error, continue using erroneous antenna?

A possible solution:

Discard erroneous antenna, and
only use remaining error-free ones



Extensive error, SDDR = 0 dB



Antenna outage

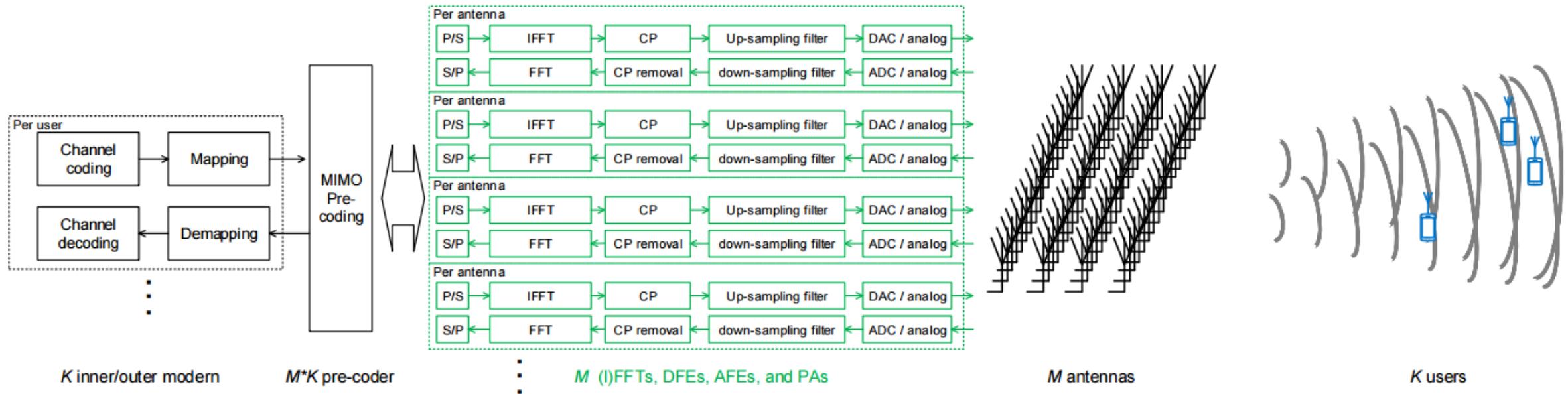
Conclusions

Massive MIMO absorbs distortions from digital error

- 40% power consumption saving possible with 1dB degradation.
- Use on-chip monitors to detect & adjust hardware failures on-the-fly.
- When hardware error distortion is
 - low, e.g. 0 dB, should continue using the erroneous antenna;
 - high, adjust the environment, or discard the erroneous antenna.

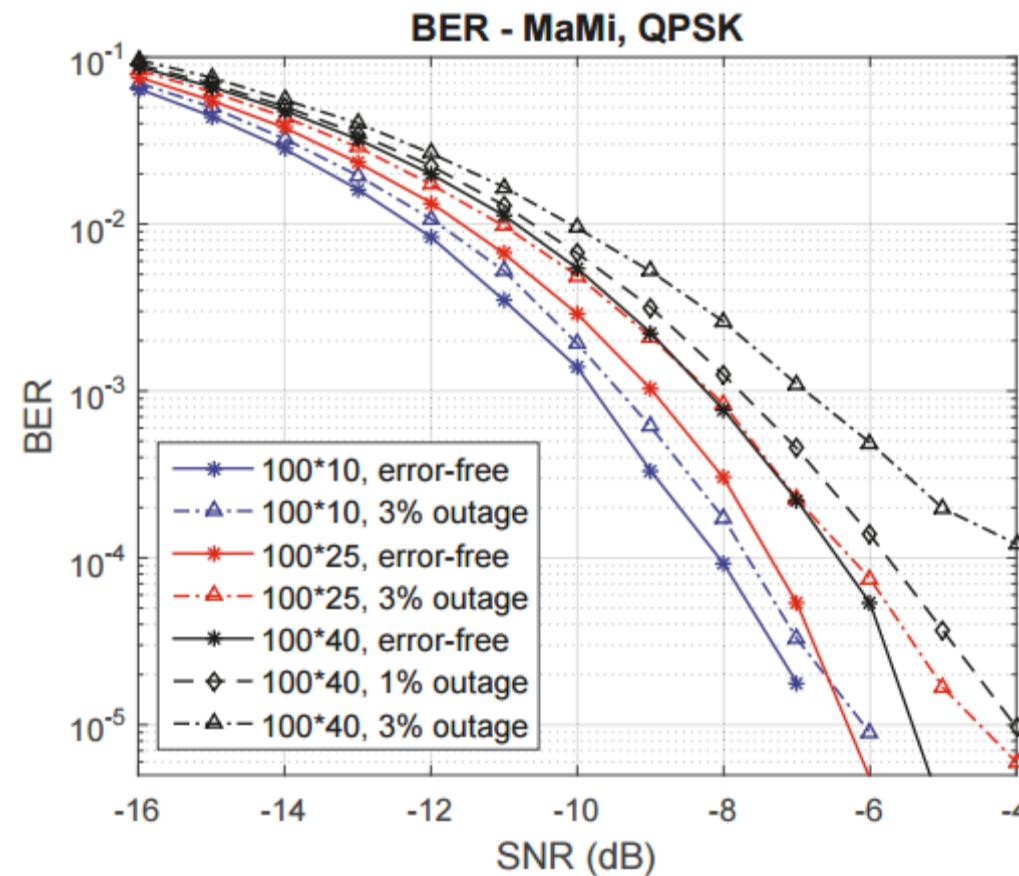
Q & A

Backup system



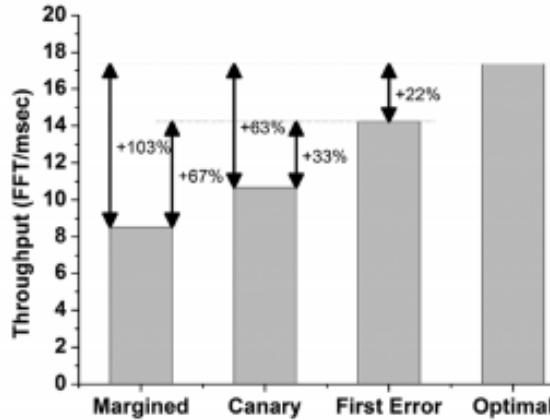
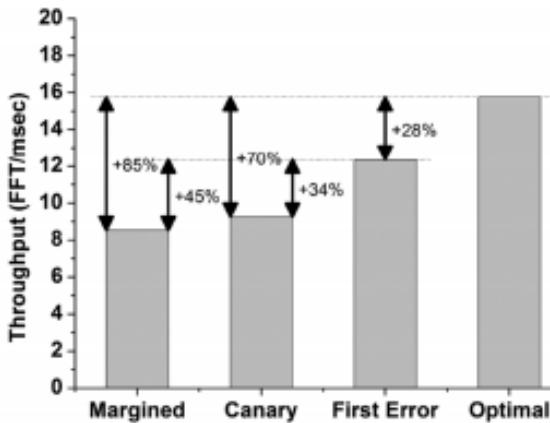
System model of the MaMi system. Each BS is equipped with M antennas and serves K users. Typically, $M = 100$ and $K = 10$.

Backup load



Backup load

Slow
Die



Avg.
Die

Fast
Die

