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FPGA Hardware Design for Plenoptic 3D Image Processing Algorithm Targeting a Mobile Application

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Agenda

1. Introduction
2. Plenoptic camera system
3. Depth estimation algorithm
4. FPGA hardware design
5. Results
6. Conclusion

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1. Introduction

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Introduction

- Plenoptic camera for depth estimation
- Mobile application
  - Smart wheeled walker for elderly
  - Warns against potential dangerous situation
- A modified depth estimation algorithm is presented
  - Works directly on the raw image
  - Calculates depth from one frame
- General purpose processors
  - Slow because of the sequential nature
- Desktop GPU is not feasible for a mobile application
  - High energy consumption
- FPGA hardware solution is presented in this study
  - To optimize execution time
  - To meet energy requirements

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2. Plenoptic Camera System

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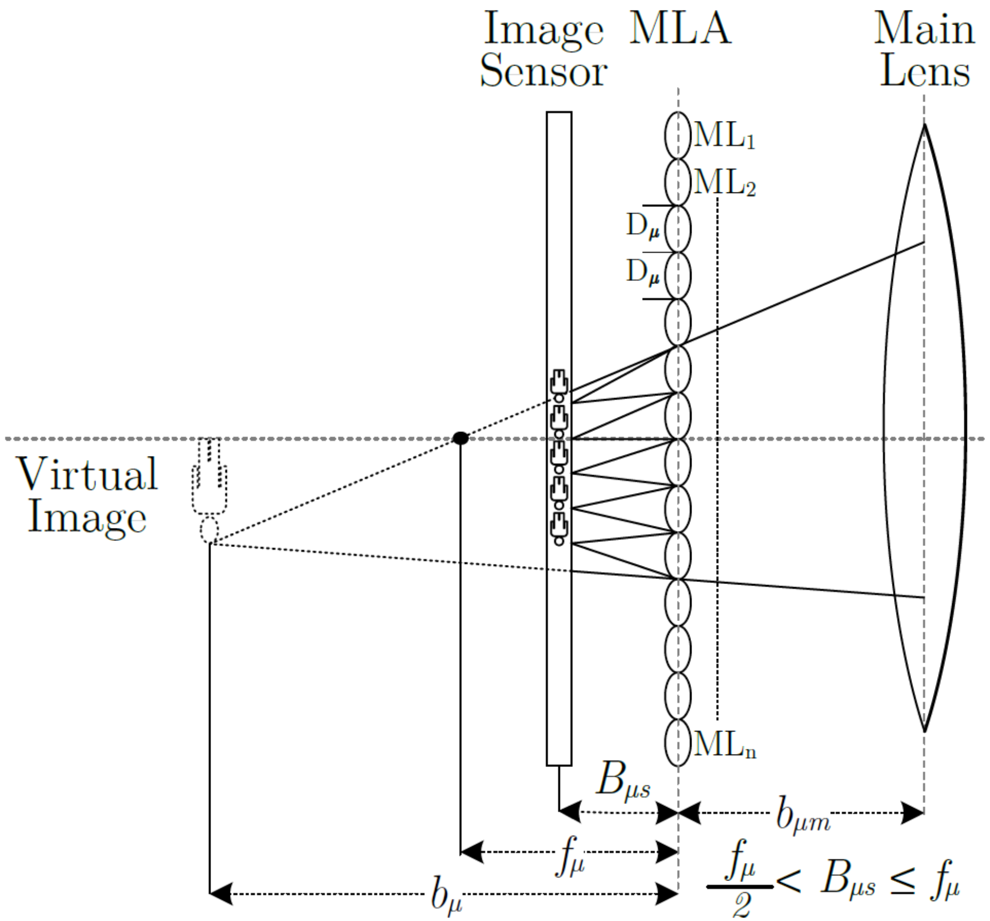
Plenoptic Camera System

- Light field camera
  - Detection of different light beams
  - From same object / scene
- MLA (micro lens array)
  - Partial images of scene
  - Different perspectives
- Advantages:
  - ✓ Single recording sensor
  - ✓ Depth estimation
  - ✓ Rectified image
  - ✓ Refocusing after capturing the scene
  - ✓ Smaller occlusion areas



(a) Raw Image

(b) Focused Image

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3. Depth Estimation Algorithm

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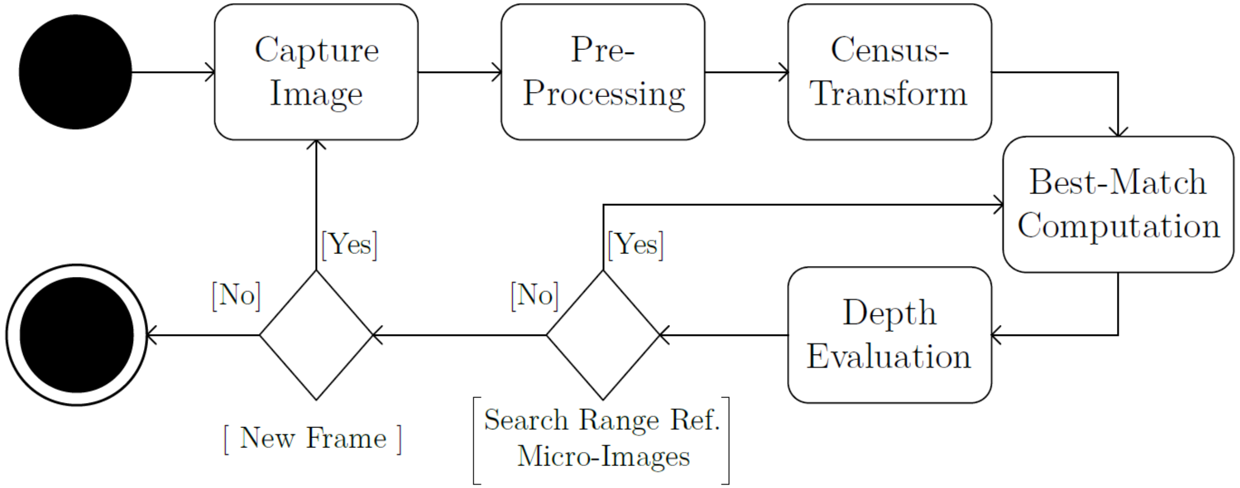
Depth Estimation Algorithm

- Virtual depth is calculated
  - Estimated distance b_μ related to B
  - $v = \frac{b_\mu}{B}$
- Virtual depth estimation is a multi-view stereo problem
- Pixel correspondences is calculated using **Census Transform**



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4. FPGA Hardware Design

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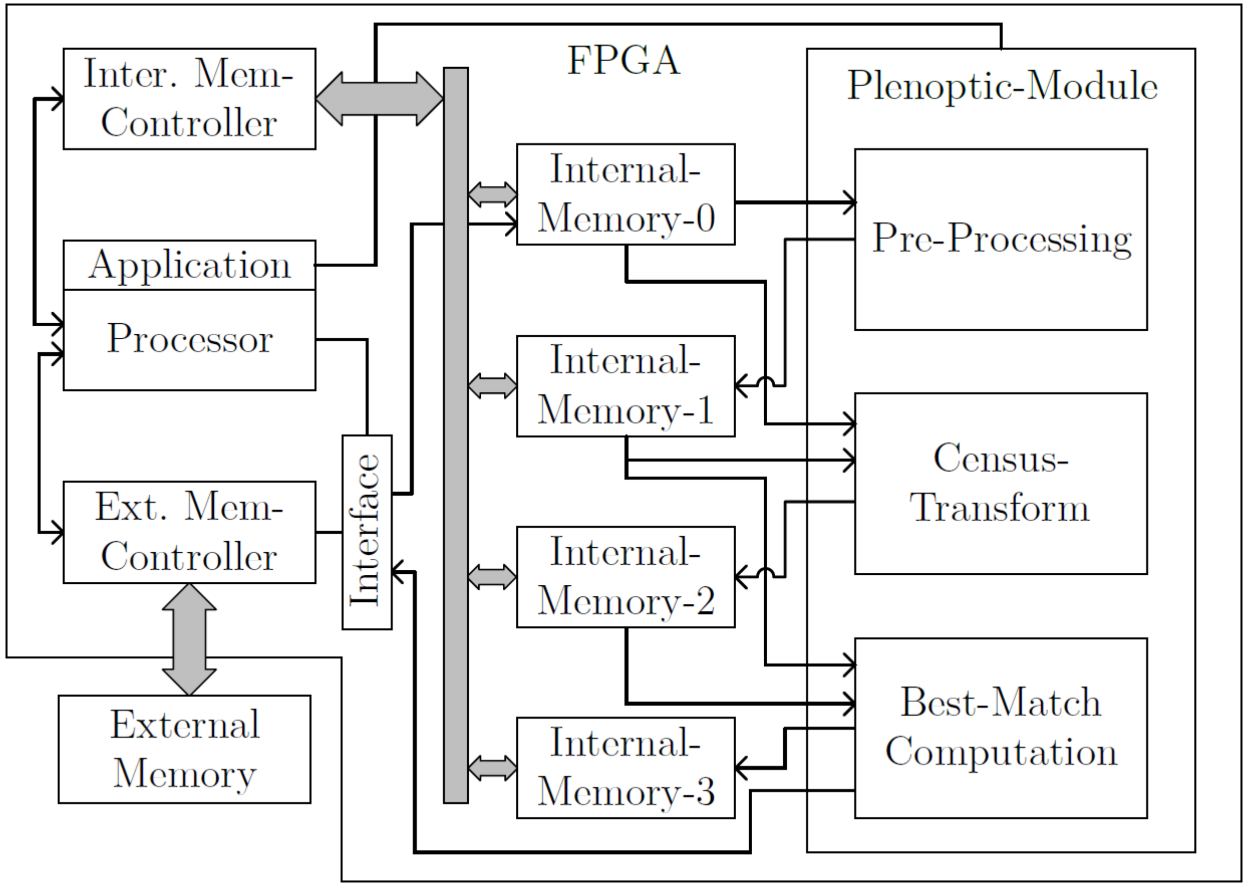
FPGA Hardware Architecture

- Plenoptic-Module
  - Pre-Processing
  - Census-Transform
  - Best-Match Computation
- Connected with internal fast memory
  - Used as a buffer
  - Limited in size
- Processor is responsible:
  - Initialization
  - Configuration
  - Data movement



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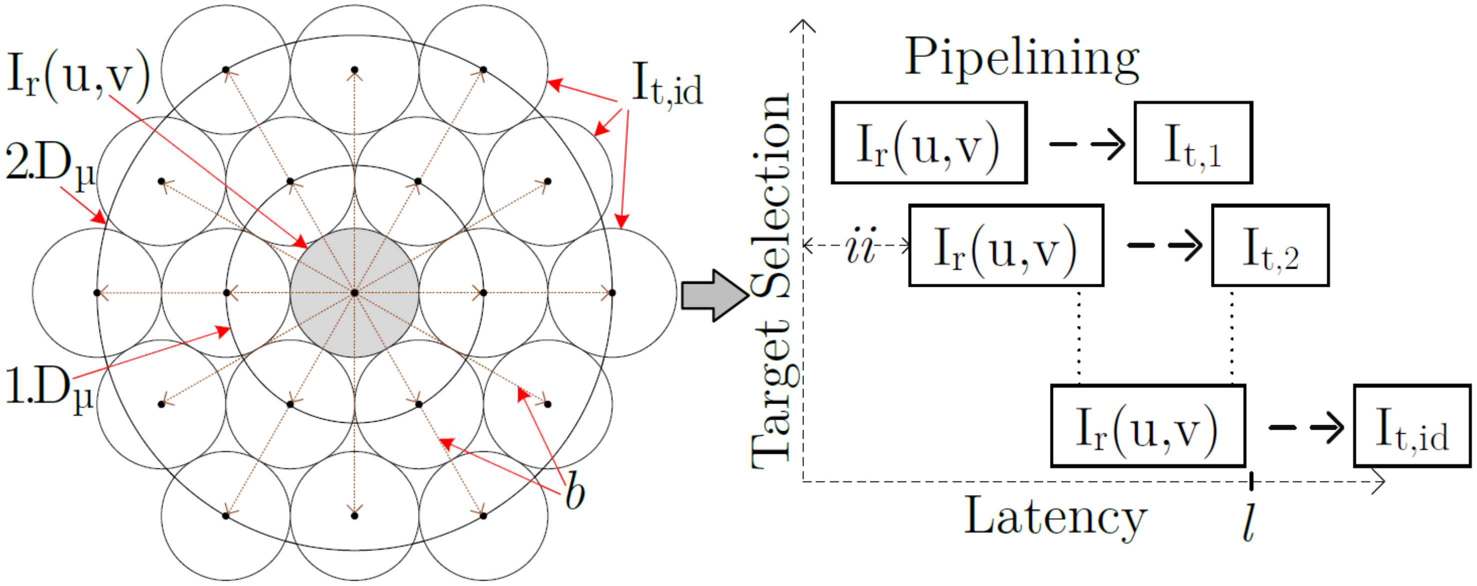
Pipelining

- Major performance bottleneck in the algorithm
  - Recursive operations to calculate depth
  - Searching for the best match of the reference pixel in neighborhood
- Number of micro-images for the matching is restricted by the baseline distance
  - Maximum baseline distance = $4.D_{\mu}$
- Concurrent selection of target micro-images



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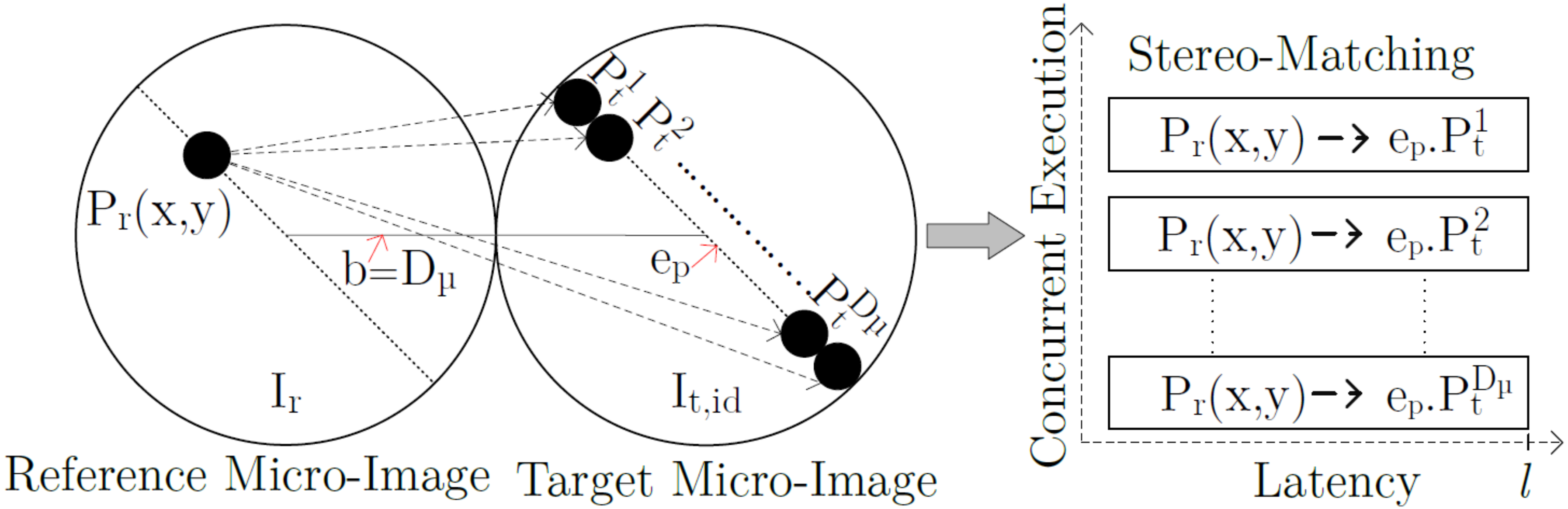
Spatial Parallelization

- After selecting target micro-image
  - Correspondence is searched within its physical boundaries
  - Micro-image is of a small size, e.g., diameter = 23 pixels
- Matching effort is reduced by limiting the search to the epipolar lines only
- Spatial parallelization is employed in the stereo-matching



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5. Results

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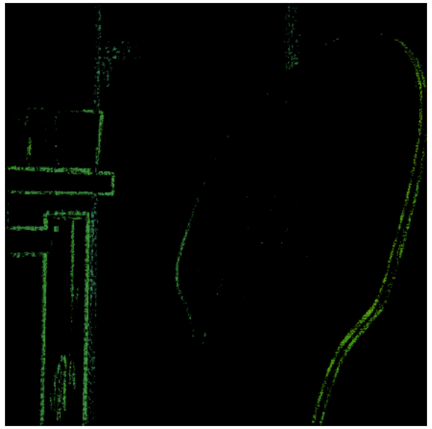
Results

- Indoor scenario: the camera is mounted on top of a wheeled walker
- Depth map computed by proposed algorithm is more dense than the RxLive

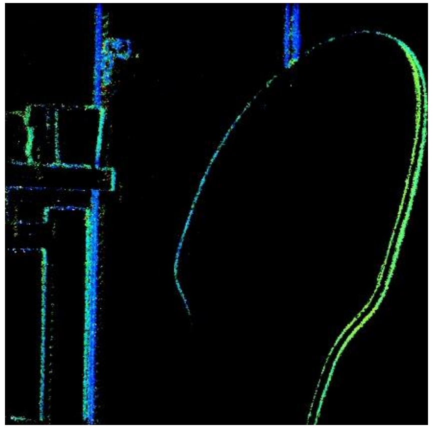
(a) Raw Image

(b) Focused Image

(c) RxLive Depth Map



(d) Proposed Algorithm



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Results

- Utilization results are calculated from HLS
- Execution time is measured per frame
- *Combination* corresponds to pipelining and spatial parallelization
- ***≈22.2x*** faster

PC-System	Intel Core i7 processor
Mobile GPU	NVIDIA Jetson Xavier NX
FPGA MPSoC	Xilinx ZCU102

- FPGA:
  - **≈ 20% faster** than mobile GPU
  - **≈ 69% faster** than PC-System
  - **Highest** fps
  - **Lowest** power consumption

Table 1: Plenoptic algorithm utilization and execution time

	Utilization				FPGA Exec. time in ms
	LUTs	**FFs**	**DSPs**	**BRAMs**	
Pipelining	14845	19094	15	10	604.1
Combination	20900	25150	13	5	334.4
Final	29412	28769	272	1797	27.2

Table 2: PC-System, mobile GPU and FPGA implementation

	Exec. Time per frame	**Throughput in fps**	**Power in watts**
PC-System	88 ms	11	60
Mobile GPU	34 ms	29	13.5
FPGA MPSoC	27 ms	36	7.1

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6. Conclusion

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Conclusion

- This study presents a modified depth estimation algorithm
  - Works directly on the raw image
  - No intermediate processing is required
- The algorithm entails challenges
  - Consists of a large number of operations
  - Requires a substantial amount of resources
- General purpose processor based solution
  - Slow because of sequential execution
- Desktop GPU based solution is not feasible in a mobile application
  - Because of high energy consumption
- This study presents optimized FPGA based solution to improve the execution time
  - The design is realized and the respective results show that the proposed FPGA hardware is faster and energy efficient

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Thank you for your time!

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