FPGA Hardware Design for Plenoptic 3D Image Processing Algorithm Targeting a Mobile Application

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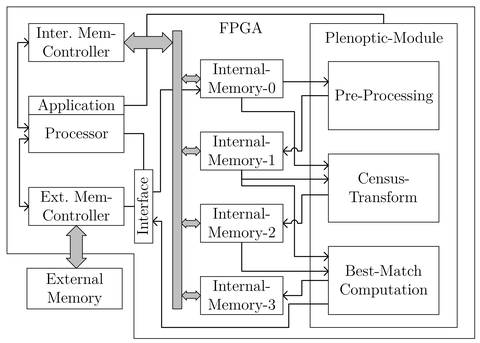
Abstract

Over the past years, widespread use of applications based on 3D image processing has increased rapidly. It is being employed in various fields, such as research, medicine and automation. Plenoptic camera system is used to capture light-field that can be exploited to estimate the 3D depth of the scene. The respective algorithms consist of a large number of computation-intensive instructions. It eventually leads to the problem of large execution time of the algorithm. Moreover, they require substantial amount of memory cells for the storage of intermediate and final results. Desktop GPU based solutions are power intensive and therefore cannot be used in the mobile applications with low energy requirements. The idea presented in this paper is to use the FPGA based hardware design to improve the performance of a 3D depth estimation algorithm by utilizing the advantage of concurrent execution. The algorithm is implemented, evaluated and the results show that FPGA design reduces the respective execution time significantly.

FPGA Hardware Architecture



- Plenoptic-Module consists of three sub-modules.
- Sub-modules are connected with *internal-memory-n* (IM-n) instances available in an FPGA device, such as low latency block RAMs (BRAMs).
- They are exploited as buffers.
- The processor ensures data mobility from external memory to the internal memory and vice versa.

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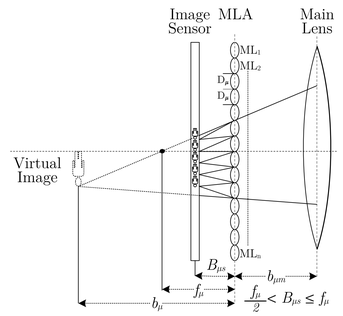
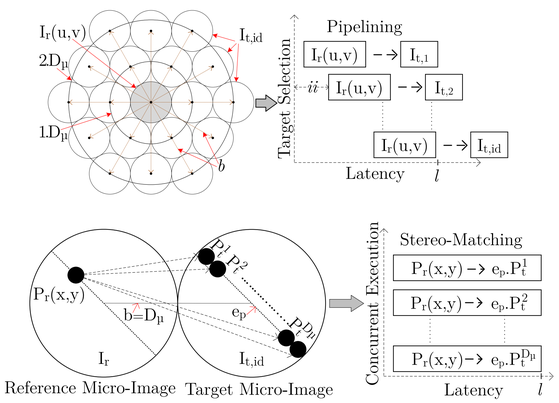
Plenoptic Camera System



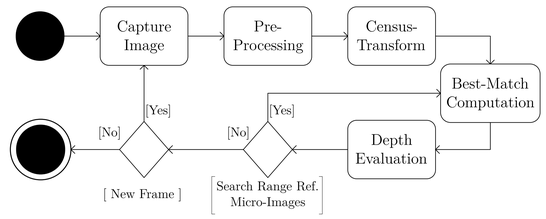
- Plenoptic camera setup is configured in a typical Gallelian mode.
- It collects light-field information of a scene by using specialized design.
- It contains *micro lens array* (MLA) between the main lens and the image sensor.

Hardware Design Optimizations



- Major performance bottleneck is caused by recursive operations to calculate the depth.
- The number of micro-lenses to find the correspondence is fixed and pipelined.
- Searching for a match within the micro-image is restricted by the physical boundary of the lens and epipolar geometry.
- Best match search within the micro-image employs spatial parallelization.

Depth Estimation Algorithm



- The proposed modified algorithm uses census transform and hamming distance to find the correspondence in stereo matching.
- *Depth evaluation* (DE) sub-module computes virtual depth v, which is a unit less relative distance to $B_{\mu s}$.

$$v = \frac{b_\mu}{B_{\mu s}} \Rightarrow v = \frac{b}{\Delta d}.$$

Evaluation

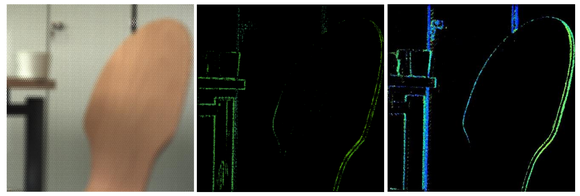


Figure: Raw image (left), RxLive depth map (middle) and depth map (right) calculated by the presented algorithm

Table: Plenoptic depth estimation algorithm utilization and execution time results.

	Utilization				FPGA Exec. time in ms
	LUTs	FFs	DSPs	BRAMs	
Pipelining	14845	19094	15	10	604.1
Combination	20900	25150	13	5	334.4
Final	29412	28769	272	1797	27.2

Table: PC-system, mobile GPU and FPGA comparison.

	Exec. Time/frame	Throughput in fps	Power in W
PC-System	88 ms	11	60
Mobile GPU	34 ms	29	13.5
FPGA MPSoC	27 ms	36	7.1

- FPGA hardware design is fastest and most energy efficient.