An Efficient Rate Control Scheme for Low Hardware Complexity Video Compression Systems

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Outline

- Lightweight Compression Introduction
- Proposed Rate Control Scheme
- Experimental Performance
- Conclusion & Outlook

Lightweight Compression Introduction

- Larger resolution & Higher spatiotemporal fidelity

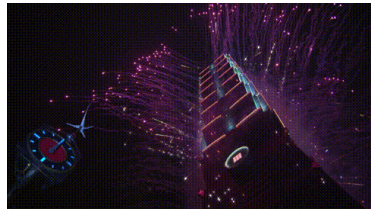
YUV 4:4:4 / RGB 4:4:4

HD

1.5Gbps

1920x1080,
30fps, 8bits

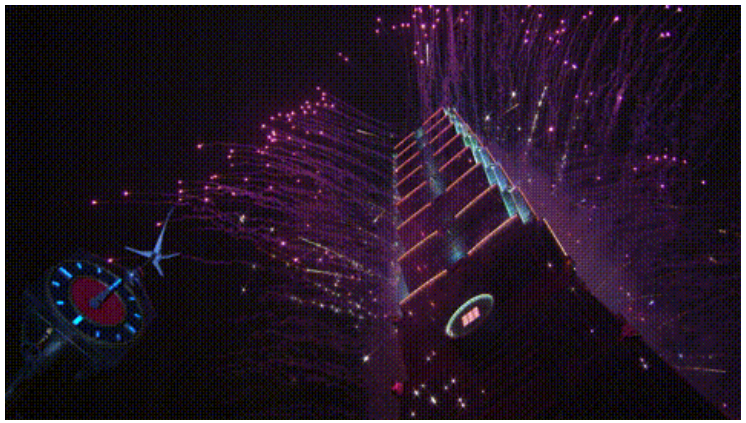
UHD-1: 4K



7.5Gbps

3840x2160,
30fps, 10bits

UHD-2: 8K



60Gbps

7680x4320, 60fps, 10bits

?

Demands drive technology evolution

Lightweight Compression Introduction

- Expensive integration upgrade

	HDMI2.0	HDMI2.1	DP1.4	DP2.0	Thunderbolt 3
Release Date	2013-09	2017-11	2016-02	2019-07	2015-06
Max Link Bandwidth	18.0Gbit/s	48.0Gbit/s	32.4Gbit/s	80Gbit/s	40Gbit/s
Max Payload Bandwidth	14.4Gbit/s	42.6Gbit/s	25.92Gbit/s	77.3Gbit/s	-

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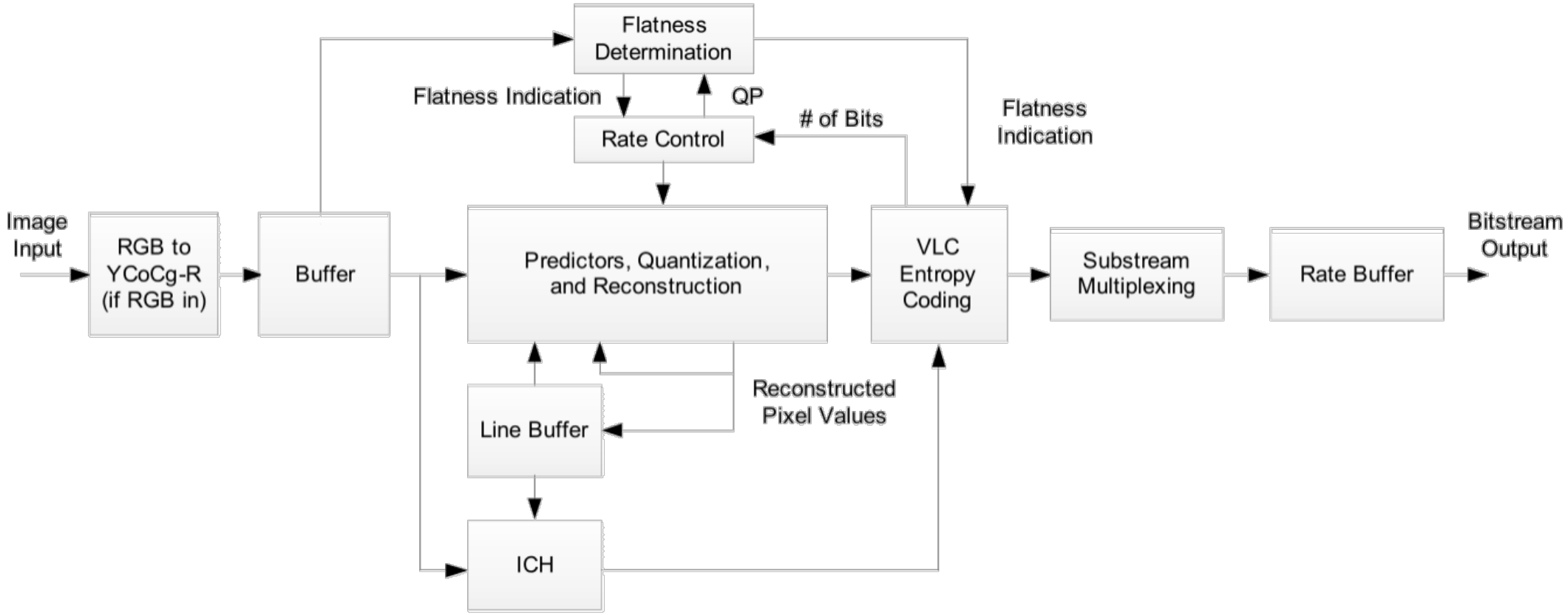
HDMI2.1	8M Pixels	11M Pixels	33M Pixels	44M Pixels
DSC			**8K@ 100/120**	**10K@ 48/50/60/ 100/120**
Lossless	4K@ 48/50/60/ 100/120	5K@ 48/50/60/ 100/120	8K@ 48/50/60	

Lightweight Compression Introduction

- Display Stream Compression
  - 3×1 process unit / only 3 predictors / decoder-side exportable params / …



Lightweight Compression Introduction

- Bottlenecks in low hardware complexity video compression systems

  - Confined on-chip context buffer
  - Compact decision clocks
  - Efficient resource allocation

Performance Upgrade

  - Larger Processing Unit
  - More Contextual Information
  - Enriching predictors …

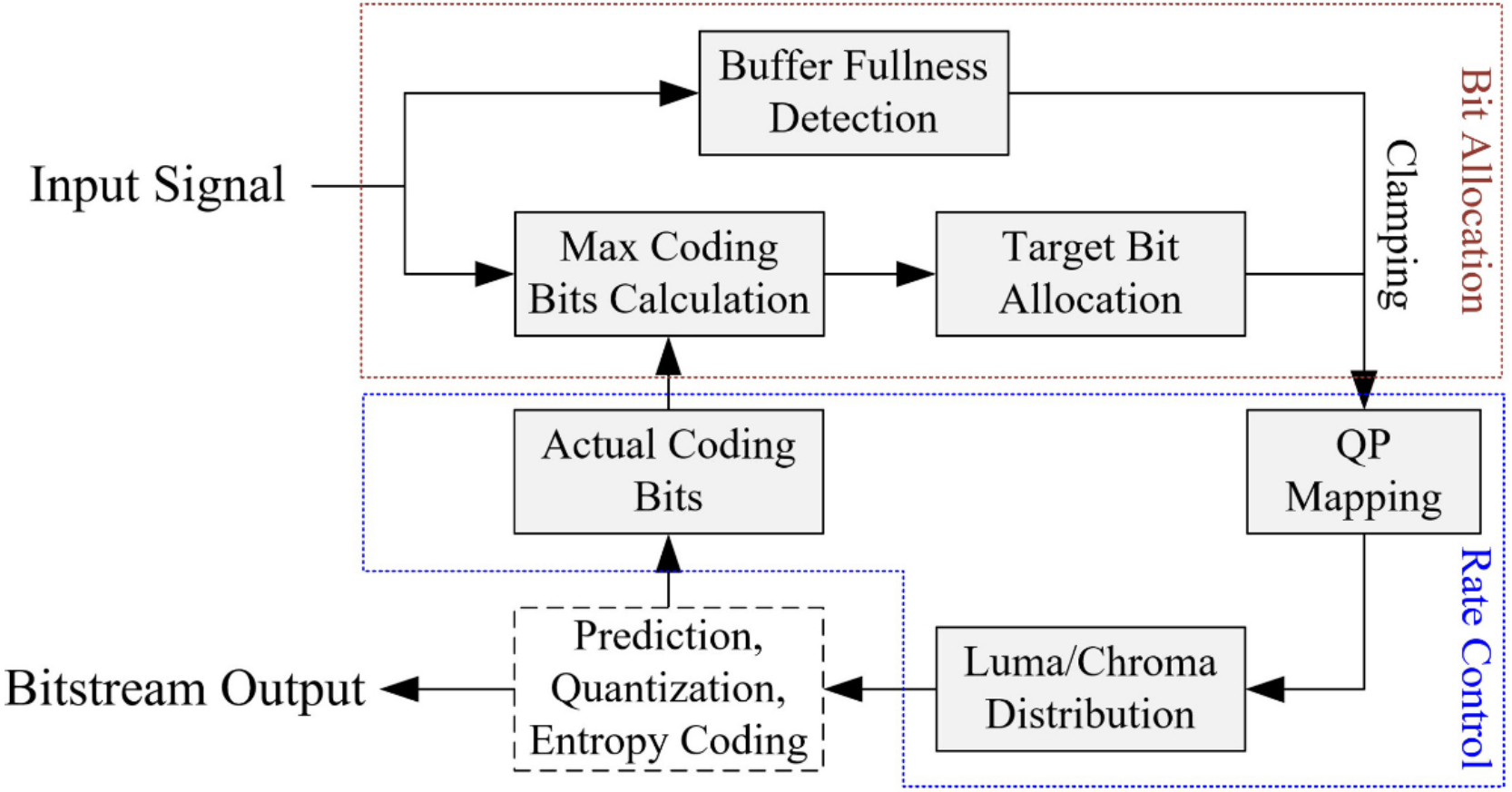
Keeping ASIC Acceptable

Bitrate Control Scheme

- Resource allocation
- Rate-distortion decision
- Quantization

Proposed Rate Control Scheme

- Rate Control Framework



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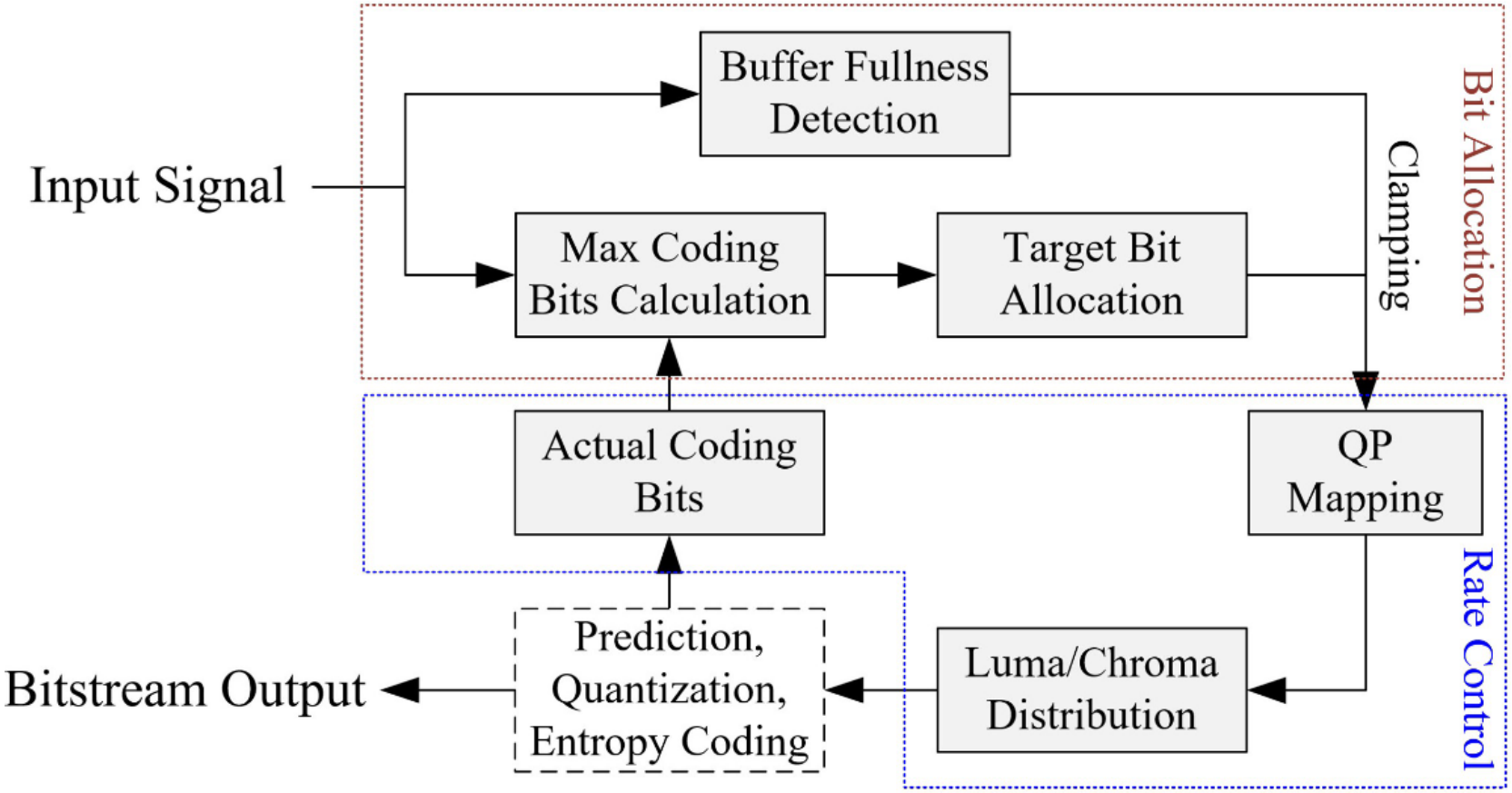


$$\sum_{i=1}^{N} \min(\nabla f_{hor}(i), \nabla f_{ver}(i)) \xrightarrow{\theta_{sp}, \theta_{cp}} level_{sub}$$

$$\Downarrow$$

$$B'_{level} = \alpha \cdot B_{level} + \beta \cdot B_{real}$$

$$\Downarrow$$

$$B = \delta \cdot bpc \cdot \frac{B' - \sigma_0}{B_{avg}} + \sigma_1$$

$$\Downarrow$$

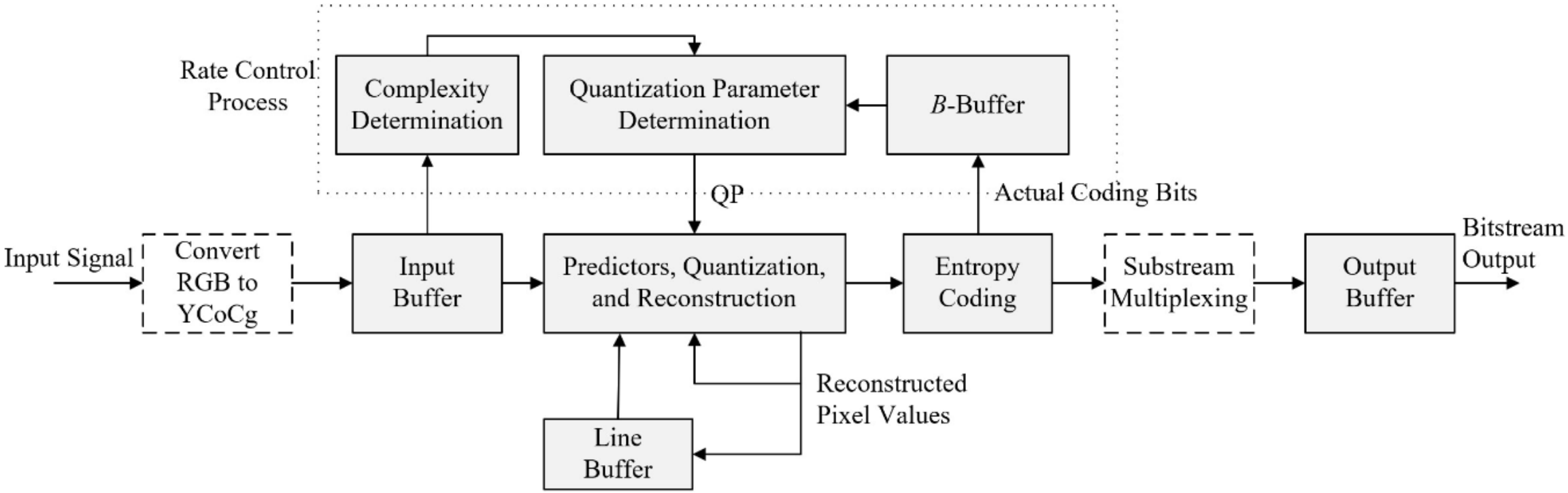
$$R \propto (\mu \cdot \log(Q_{step} + 1) + \varphi)$$

$$\Downarrow$$

$$\mathrm{QP}_{Luma} \ \& \ \mathrm{QP}_{Chroma}$$

Experimental Performance

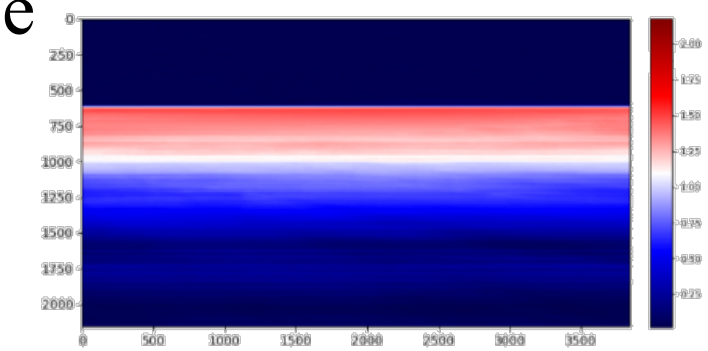
- Experimental platform
  - 16×2 coding unit / more predictors / less stream buffer / non-ICH framework



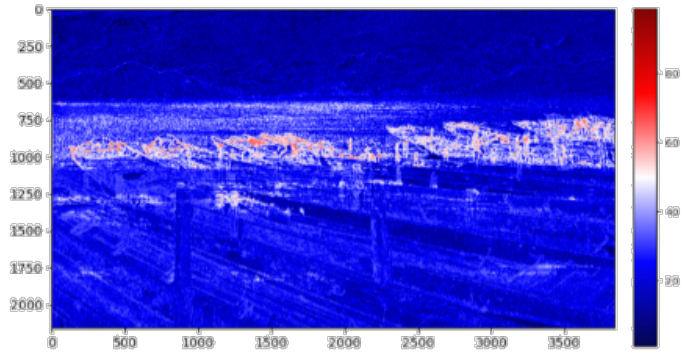
Experimental Performance

- Rate Control performance

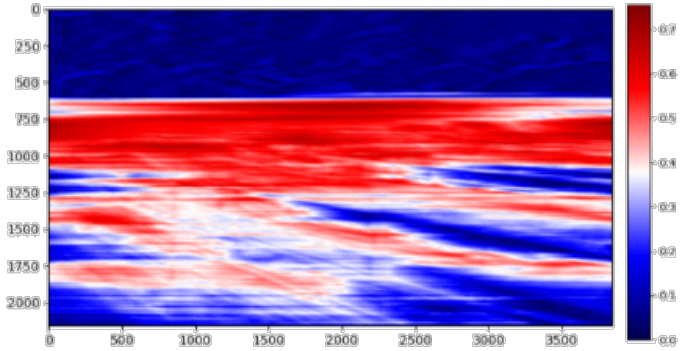
(a) Input Signal (3840×2160 YUV4:4:4 12-bit)



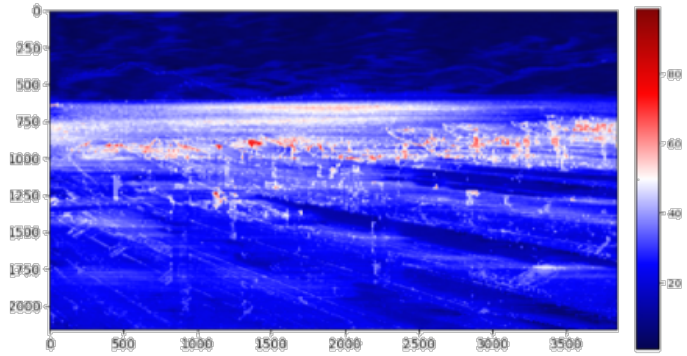
(b) DSC Buffer Fullness 100% = 8192 bits



(d) DSC Q-step



(c) Proposed Buffer Fullness 100% = 8192 bits



(e) Proposed Q-step

Conclusion & Outlook

- We proposed an efficient rate control scheme for low hardware-complexity video compression systems, especially for ASIC-oriented codec, which performs more flexible and aggressive.
- The proposed rate control scheme is believed to support larger coding units and more complex decision logic in display stream compression.
- More experiments and comparisons will be studied. More optimized rate control strategy and mentioned coding platform have being investigated.

Thanks

An Adaptive Intra-Frame Quantization Parameter Derivation Model Jointing with Inter-Frame Analysis

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