An heterogeneous compiler of dataflow programs for Zynq Platforms

Endri Bezati\textsuperscript{1} Simone Casale-Brunet\textsuperscript{1} Romuald Mosquera\textsuperscript{1} Marco Mattavelli\textsuperscript{2}
\textsuperscript{1}EPFL VLS, \textsuperscript{2}EPFL SCI STI MM, École Polytechnique Fédérale de Lausanne, Switzerland
\textsuperscript{3}School of Business and Engineering Vaud HES-SO, REDS Institute at HEIG-VD, University of Applied Sciences Western Switzerland, Yverdon-les-Bains, Switzerland

In recent years, the number and variety of heterogeneous multiprocessor system-on-chip MPSoCs, such as for instance Zynq platforms, has sensibly increased. However, today all design flow solutions capable of programming the different components of such platforms require to the designer either to modify the software or hardware based designs to obtain higher performance implementations. Thus, the developer needs to either rewrite functional blocks in HDL or to use high-level synthesis of C-like sequential languages with platform locked extensions. In this paper, a compiler infrastructure that takes as input a single behavioral representation, expressed in high-level dataflow RVC-CAL language, is proposed for programming any of the components of heterogeneous Zynq MPSoCs platforms without the need of modifying any line of code on the design.

The RVC-CAL Dataflow Language

RVC-CAL is a high level dataflow language adopted by MPEG for its Reconfigurable Video Coding Initiative. It is structured around the concepts of: Actors, Actions, Finite State Machines and Procedures.

Architecture

The architecture defines on which kind of platform the design is implemented. The architecture contains operators, media, and links, which is described in the XCF file.

HW-SW Interfacing

How actors communicate with each other, when partitioned between the Processing System (PS) and Processing Logic (PL) of the Zynq MPSoC.

Decoder performance on the ZedBoard

Decoder output throughput in MHz

P1 P2 P3 P4 P5 P6 P7 P8
0 10 20 30 40 50 60

Vivado block design representation of the P8 partition, all generated actors and interface IP blocks are instantiated automatically.